# A Vcm-based 11-bit 20MS/s Noise Shaping SAR ADC with 4× Passive Gain

## 一具有四倍增益之雜訊整形的共模電壓基底每秒兩千萬次採樣之十一位元的連續漸近式類比轉換器

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## Abstract

**Analog-to-Digital Converter (ADC) is a key circuit that converts analog signals into a digital form. Particularly, Successive Approximation Register (SAR) ADC features low power and moderate resolution, but suffers from limited resolution and quantization noise.**

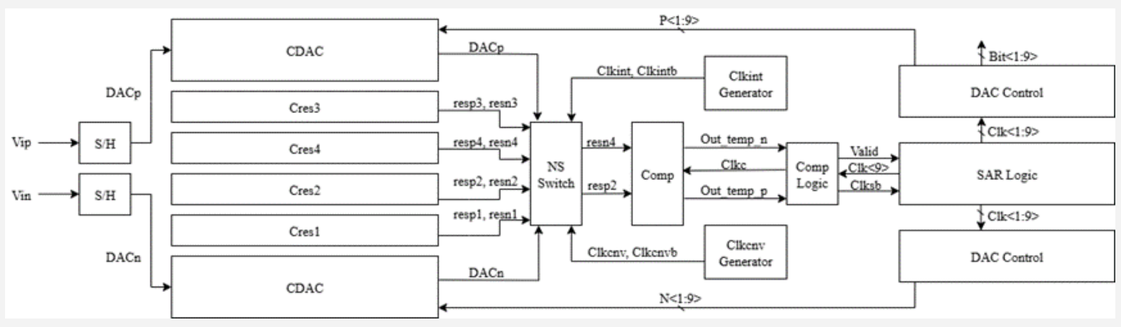
**This project is based on J.Liu ISSCC 2020, which enhances the performance of pure SAR ADCs by implementing a Noise Shaping (NS) structure. This architecture achieves 4× passive gain and residue integration. Although the input range of the ADC slightly decreases, our project maintains low power and high resolution across all process corners. In summary, this project demonstrates a NS SAR ADC with noise shaping capability, effectively suppressing quantization noise.**

## Circuit Structure

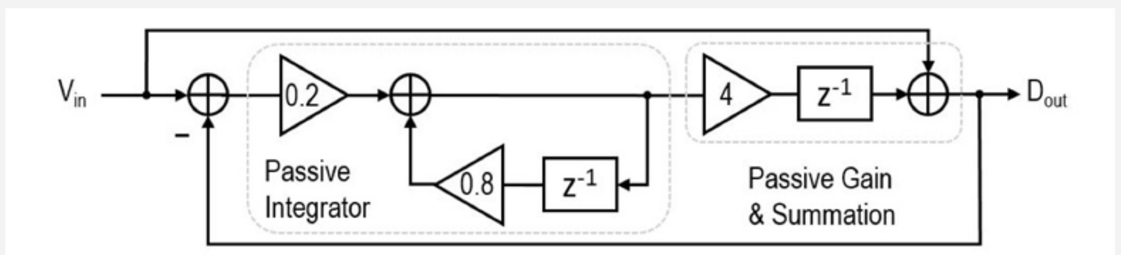
**Fig.1 is the block diagram of the project. The differential inputs are processed by a Sample-and-Hold (S/H) circuit. This circuit delivers sampled input signals to the top plates of the Cdac arrays while the clock is high and holds when the clock is low. The ADC then enters the conversion phase. Clkcnv is pulled high to control the NS switch. This lets the signal on DACp and DACn be summed with the residue from the previous cycle. Later, Clkc is pulled high through the SAR logic control circuit to enable the Strong-Arm Comparator. The comparator yields the outputs. The top-plate-sampling method is adopted to eliminate the first-round comparison.**

**S/H Circuit is especially examined for its pre-sim and post-sim results to make sure it can sample 13 bits effectively. Likewise, StrongArm Comparator is designed to meet specific speed and noise limit, so that the output is sufficiently correct. In the asynchronous clock control circuit, we use the output of the comparator to activate TSPC. This creates clocks with different trigger times. It also ensures the next comparison is available only after the current round is completed.**

**After comparison for 9 rounds, Clkint is pulled high for residue integration. In the integration phase, the 4 Cres capacitors are connected to the top plates of Cdac to store the difference between them. The residue will be added to the comparator input in the conversion phase in the next cycle. The outputs of the comparator will be sent to latch and DAC Control, yielding Bit<1> to Bit <9>. With the above process, a cycle of Analog-to-Digital Converting is finished. Fig.2 illustrates the signal flow. Finally, we use MATLAB code to read in 9-bit signals, calculate, and confirm the circuit performance.**




▲ Fig. 1: ENOB 11-bit Noise Shaping SAR ADC Block Diagram




▲ Fig. 2: Signal Flow Graph [1]

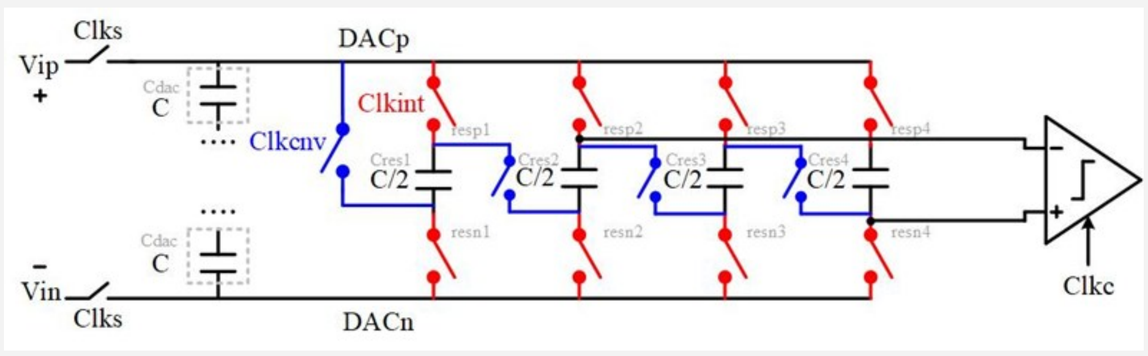
## Noise Shaping Architecture

**This project features NS architecture to alleviate quantization noise. This concept combines the SAR and the DSM: power efficient and low cost as SAR, and high SNR as DSM.**

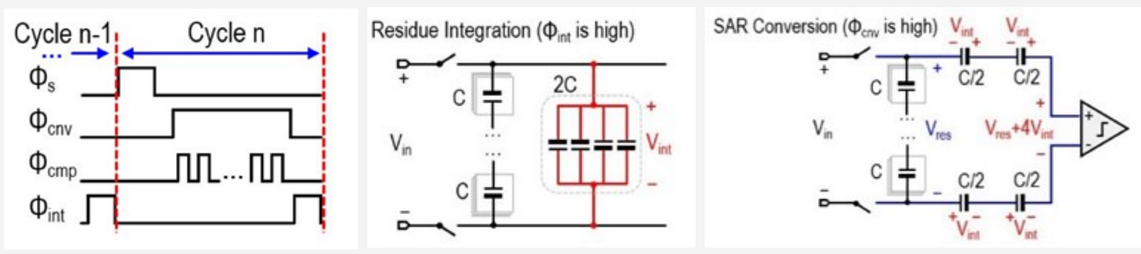
**In a conventional SAR ADC, the finite DAC resolution leaves a residue, which is also referred to as the quantization error, between the analog input and the DAC output at the end of conversion. This residue is shaped in NS SAR architectures using either an Error-Feedback (EF) or a Cascaded-Integrator Feed-Forward (CIFF) loop filter, and this work adopts the CIFF structure.**

**Fig.3 shows the schematic of the NS switch and Cres, and Fig.4 demonstrates the working principle of noise shaping. In the current cycle, the residue of the Cdac top plates will be sampled and preserved by the 4 Cres to achieve residue integration, called Vint. Later, in the next cycle, the residue will be added to the input of the comparator, creating the input voltage difference of Vres + 4Vint. To summarize, such capacitive stacking realizes signal summation and amplification, which can provide integer gain with high linearity.**

**We implement the NS switch with transmission gates and adjust sizes properly to reduce charge injection. By means of sample, conversion, and residue integration, we finally achieve the first order NTF = 1 - 0.8 $z^{-1}$.**




▲ Fig. 3: Schematic of Noise Shaping Structure




(a) Timing Diagram　(b) Residue Integration　(c) Residue Integration

▲ Fig. 4: Working Principle of Noise Shaping [1]

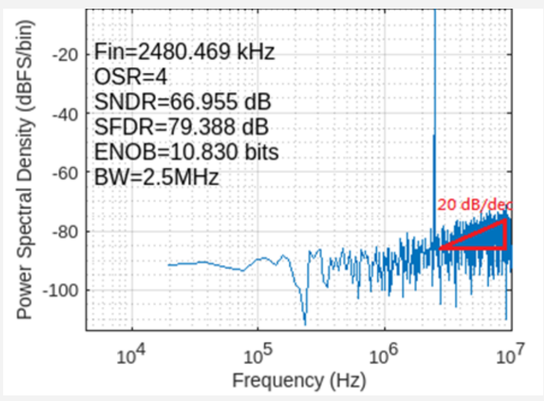
## Simulation Results

**Table 1 shows the ENOB results for the NS SAR ADC at different process corners for Pre-Sim and Post-Sim at 25°C, sampling rate of 20MHz, OSR = 4, and input range of 91%. Fig.5 presents the FFT spectrum of the output at TT 25°C, showing reasonably shaped noise, and the power consumption is approximately 0.7mW.**

(Unit: Bit)

| Corner | Pre-sim | Post-sim |
|---|---|---|
| TT | 11.0916 | 10.8298 |
| FF | 11.1041 | 10.6832 |
| FS | 11.1608 | 10.8768 |
| SS | 11.1146 | 10.6402 |
| SF | 11.0540 | 10.7747 |

▲ Table 1:
Pre-sim & Post-sim ENOB

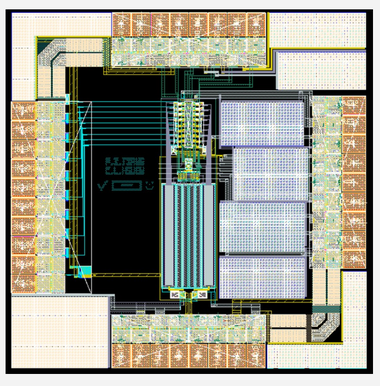



▲ Fig. 5: FFT analysis

## Conclusion

**This project demonstrates a 11-bit, 20MHz Noise Shaping SAR ADC using T18 process, integrating Vcm-based SAR ADC and Noise Shaping architecture to improve SNDR. This design verifies the feasibility of achieving both low power and quantization noise suppression.**

**Although passive capacitor stacking introduces challenges of area and order limit, the design meets the specification and validates the potential of NS SAR ADC.**



▲ Fig. 6: Layout

## References

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