Hardware-Accelerated Design for Client-Specific Trading, Account Query, and Margin Calculation in the Taiwan Futures Market

適用於台灣期貨市場之客戶特定交易、帳戶查詢及保證金計算硬體加速設計

Group:B557 **Professor:馬席彬** **Group member:孟德為、王彥凱、謝亦丞**

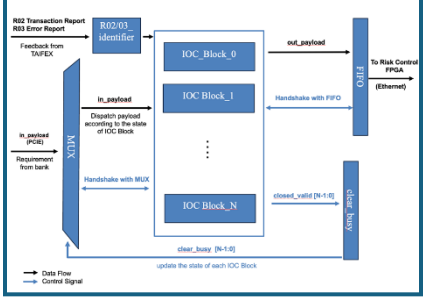
Abstract

In April 2025, the U.S. government announced new tariff measures that triggered sharp volatility in global financial markets. The resulting surge in futures trading volume caused delays and even outages in several trading systems. To address this issue, our study applies FPGA hardware to the futures trading environment, aiming to resolve the heavy load created by numerous IOC orders and frequent margin updates faced by our industry partner's software system. With its highly parallel computational capability and programmable logic architecture, an FPGA may help us enhance system reliability, performance, and resilience.

Implementation

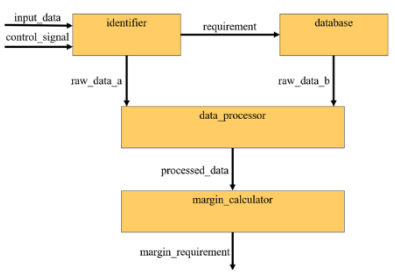
Multi-IOC Acceleration Module

The Multi-IOC Module is capable of parallel processing for high-throughput option IOC trading orders. The architecture monitors market prices to avoid unnecessary submissions, updates remaining quantities using exchange feedback, and coordinates order flow with the Risk Control FPGA. It also logs all events and handles termination conditions, achieving low-latency, scalable performance for real-time trading systems.



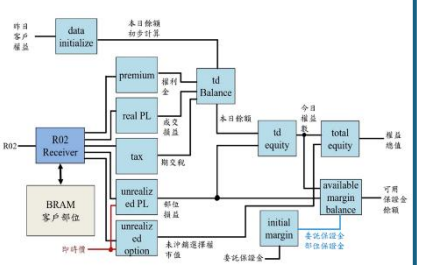
Margin Computation Module

The margin computation module encompasses the calculation of both order margins and position margins. Its core design objective is to implement, in Verilog, the margin formulas specified by the Taiwan Futures Exchange and to coordinate the data interfaces among the surrounding hardware modules. Because both the multi-IOC engine and the risk-control module depend on the outputs of this block, the detailed communication protocol between modules is particularly critical.



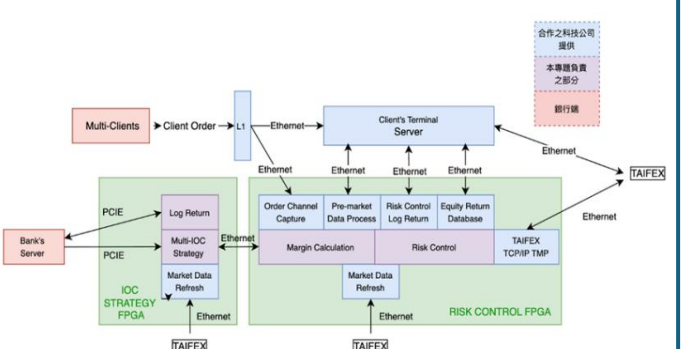
Available Margin Module

According to the regulations of the Taiwan Futures Exchange, customer account data, real-time market quotes, and position changes must be continuously integrated to update each client's margin balance. The calculated available margin indicates the amount a client can still use to open new positions or increase existing ones. This value serves as a crucial indicator of an account's risk-bearing capacity and liquidity.



System Architecture Overview

This system employs dual Xilinx Alveo U50 FPGAs to accelerate real-time trading tasks and ensure efficient order processing. When receiving a multi-IOC requirement from the bank, the IOC Strategy FPGA generates multiple IOC orders based on the requested strategy, records all related logs, and forwards the newly created orders to the Risk Control FPGA. The Risk Control FPGA receives both regular and IOC orders, performs initial-margin and maintenance-margin calculations, evaluates available margin, and determines whether each order should be accepted or rejected. Additional supporting modules, including Market Data Refresh, TAIFEX TCP/IP TMP, and other infrastructure components, are provided by an industry partner to complete the full trading pipeline. Overall, the architecture leverages FPGA parallelism to deliver high-throughput, low-latency, and risk-aware trading operations.



Conclusion

This project completes the hardware functionality and timing verification, producing a prototype system that can interface with existing matching and risk-control modules. The core components—including real-time IOC order checking, margin and equity updates, and risk reporting—are implemented using FPGA-based parallelized designs. Compared with traditional software architectures, the proposed solution handles the heavy computational load induced by volatile market conditions, significantly reduces end-to-end latency, and lowers CPU utilization

Reference

[1] Taiwan Futures Exchange (2025). Official Website. Retrieved from：https://www.taifex.com.tw/cht/index
[2] Taiwan Futures Exchange (2024). TAIFEX File Transmission Format_v1.12.0
[3] Taiwan Futures Exchange (2024). TAIFEX TCPIP_TMP_v2.18.5
[4] Taiwan Futures Exchange (2025). Tick-by-Tick Data Feed Operations Manual(V1.9.0)