A 64x64 CMOS Image Sensor Integrating 3T-APS and PWM Pixel Sensor Technology with Single-Slope ADC and 10-bit Resolution

一個整合3T-主動式像素及脈衝寬度調變像素並採用單陡坡類比數位轉換器與10位元解析度的64x64互補式場效電晶體影像感測器

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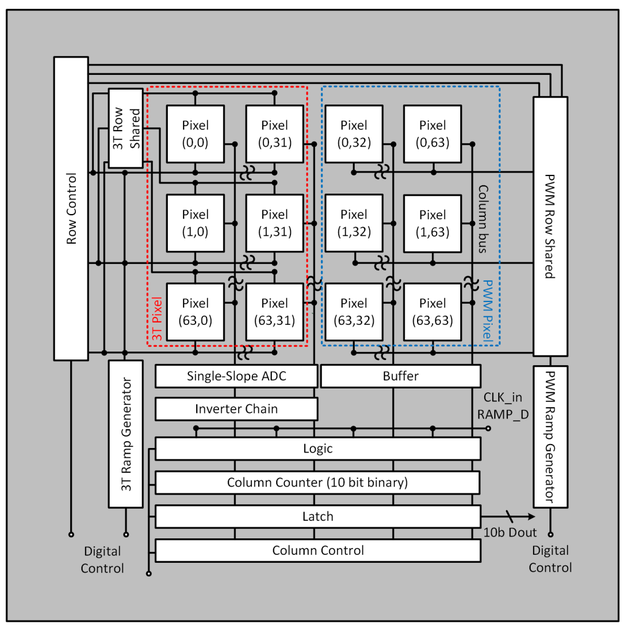
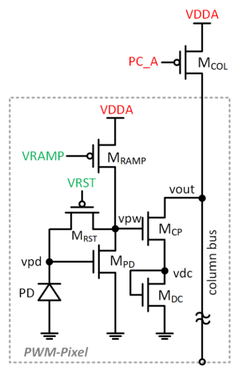
Abstract

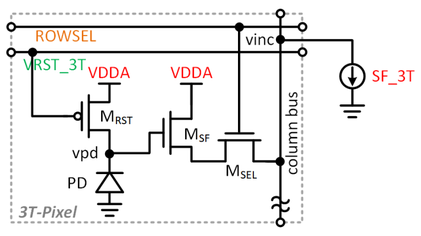
In this project, we developed a 64x64 CMOS image sensor array integrating two types of pixel sensors: the conventional 3T active pixel sensor (3T-APS), known for its simplicity and high signal-to-noise ratio, and a modified pulse-width modulation (PWM) pixel sensor. By adding a diode-connected MOS transistor to the PWM pixel circuit, we enhanced its linearity, aiming to compare the output linearity and imaging performance of both pixel types at 1.8V operation with 10-bit resolution.

Implementation

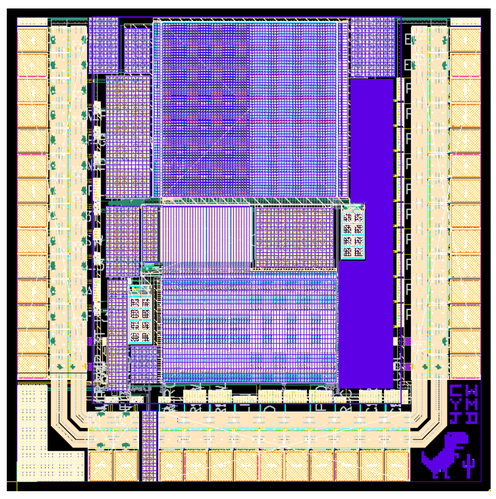
System Architecture & Pixel Circuit







Full-Chip Layout

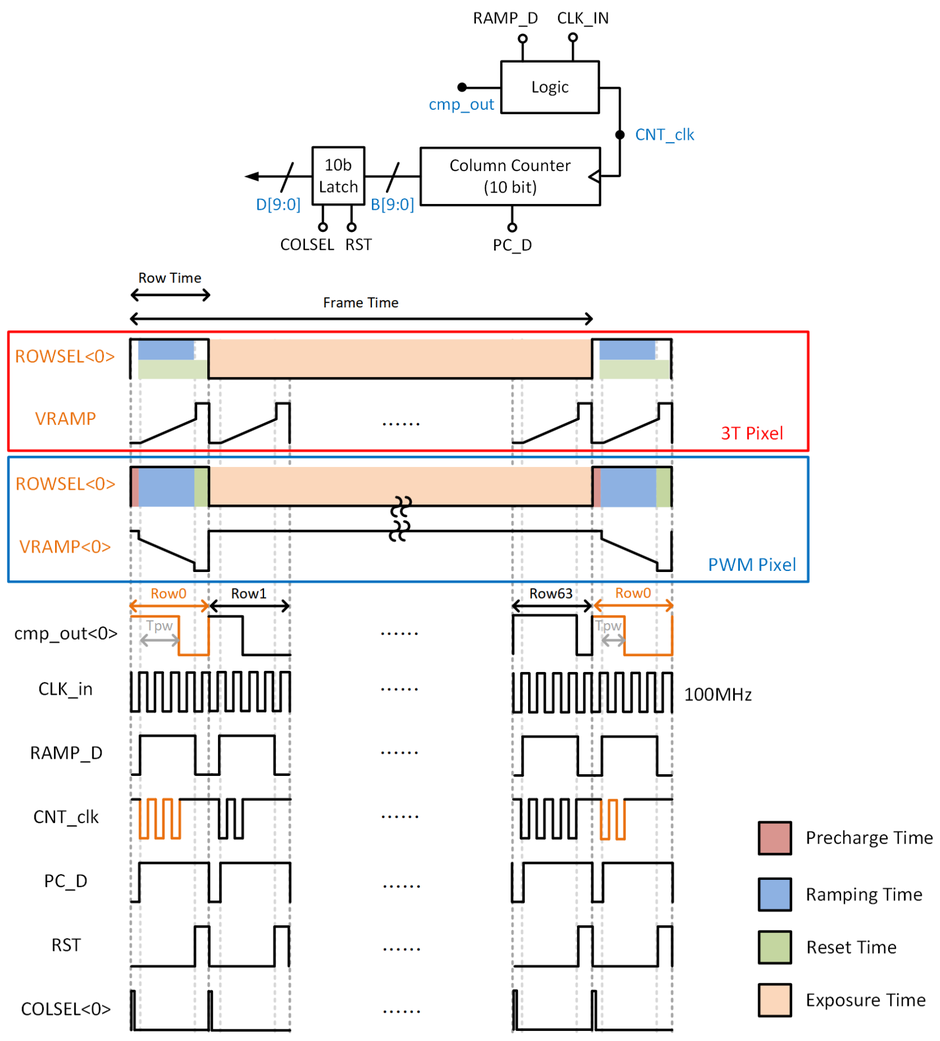


Chip Size：1200 x 1200 um^2
Transistor / Gate Count：50996 transistors

Table 1. Spec Table

	Spec	Pre-sim (TT)	Post-sim (TT)
CMOS Technology	0.18 um	0.18 um	0.18 um
Supply	1.8V	1.8V	1.8V
Pixel Array Size	64x64	64x64	64x64
Pixel Count	4096	4096	4096
Pixel Pitch (um)	7	-	7
Fill Factor	-	-	3T pixel：34.19% PWM pixel：13.63%
Counter	10-bit	10-bit	10-bit
Max. Frequency	≥ 100 MHz	100 MHz	100 MHz
Chip Size (mm^2)	≤ 1.2x1.2	-	1.2x1.2
Frame Rate (fps)	1240	1240	1240
Power Dissipation (uW)	-	2.001	2.447

Readout Operation Timing Diagram



This study adopts a rolling shutter readout method, where rowsel<n> sequentially selects each row for readout. The diagram on the left illustrates this process using row0 as an example.

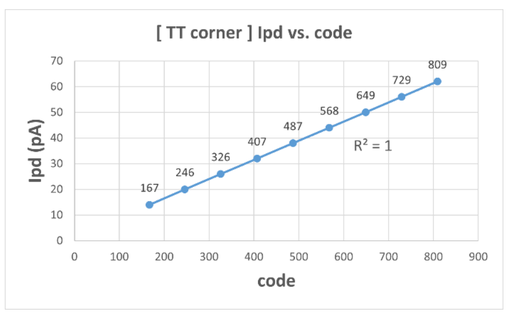
(1) **3T Pixel Operation**: The 3T pixel outputs a signal in the voltage domain. This is converted into a time-domain pulse-width signal using a single-slope ADC, where a ramping signal VRAMP serves as the input to the ADC.

(2) **PWM Pixel Operation:** For the PWM pixel, the ramping signal VRAMP<0> is directly input into each pixel, producing a pulse-width signal as its output.

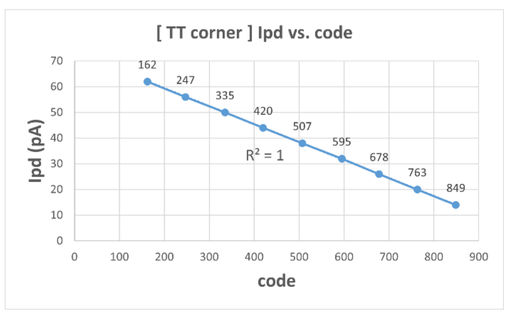
(3) **Exposure-Dependent Pulse Width:** In the 3T pixel, the pulse width increases with higher exposure levels. In contrast, the PWM pixel's pulse width decreases with higher exposure.

After these operations, each column receives a pulse width signal, cmp_out<n>, which is processed by a common column readout circuit for both pixel types. Using a 100MHz clock, a CNT_clk is defined by the Logic circuit within the cmp_out pulse range, and a column counter then converts this to a 10-bit code. The result is stored in a latch, and colsel<n> sequentially reads out each column's result from row0.

Result



3T pixel – Post-sim (TT corner)



PWM pixel – Post-sim (TT corner)

Table 2. 3T pixel - INL_bestfit results at different corners

INL_bestfit (Unit：LSB)	TT	FF	FS	SF	SS
Pre-sim	±1.40	±3.02	±1.15	±5.22	±2.24
Post-sim	±1.66	±2.66	±1.25	±6.42	±2.62

Table 3. PWM pixel - INL_bestfit results at different corners

INL_bestfit (Unit：LSB)	TT	FF	FS	SF	SS
Pre-sim	±1.52	±3.95	±2.71	±1.47	±3.31
Post-sim	±4.21	±4.43	±3.81	±3.92	±3.64

The results of this study validate the differences between the 3T pixel and PWM pixel in aspects such as linearity, circuit structure, and layout area efficiency, providing a reference for future design applications.

Reference: [1] Yen-Chih Chiou (2018). The Research of Low Voltage and Low Power Pulse- Width Modulation CMOS Imagers. National Tsing Hua University, Taiwan. [2] Jun Ohta (2008). Smart CMOS Image Sensors and Applications. London, England: Taylor & Francis. [3] Junichi Nakamura (2006). IMAGE SENSORS and SIGNAL PROCESSING for DIGITAL STILL CAMERAS. London, England: Taylor & Francis.