A Low-Noise Amplifier with V/I Converter Applied to Front-End ECG Signal Detecting Application

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ABSTRACT

This project aims to implement a low power, low noise ECG signal analog front-end (AFE) integrated circuit (IC). The gain and bandwidth are optimized based on the characteristics of the ECG signal. The high pass corner of our LNA is 300mHz, and the low pass corner is 1kHz.Also this project focuses on improving CMRR, achieving a CMRR of 176dB@50Hz in this project. The achieved input referred noise is $31.14\mu V_{rms}$ and the power consumption is 8.0952 μW with the power supply of 1V.

Keywords ECG recording front-end, Low noise, Low power, pseudo resistor, bulk input CMFB

Background

AFE is the one of the most important components in a biomedical chip. This block is positioned right after the electrodes and interfaces directly with the bio signal. Its function is to process the signal transmit it to subsequent blocks. The frequency range of ECG signal of interest is approximately 500mHz to 150 Hz.

Implementation

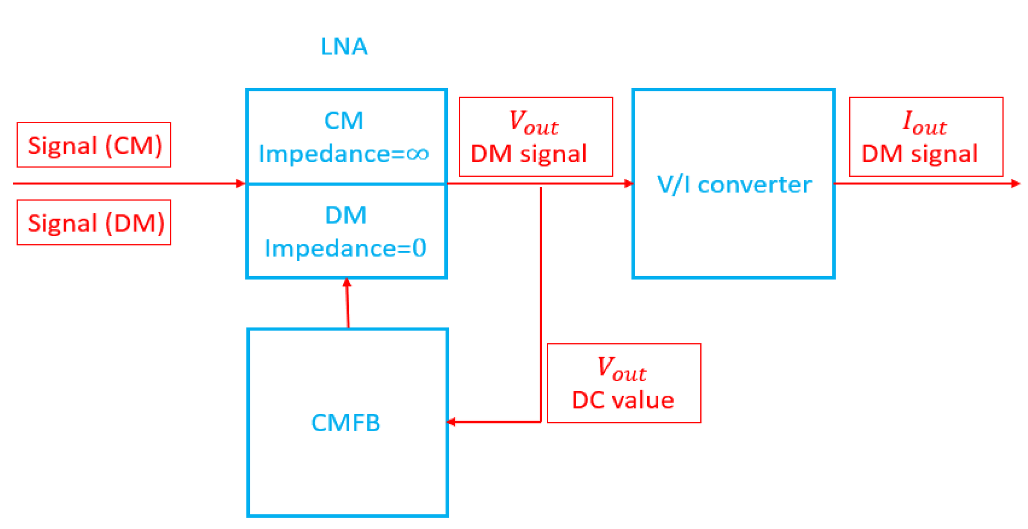

Fig 1. the block diagram of the overall structure including LNA, CMFB. V/I converter

Fig 1. illustrates the block diagram of 2 stage structure, which we will discuss separately. The first stage is the low noise amplifier (LNA) and the second stage is the voltage to current converter(V/I converter). In LNA, capacitive-resistive feedback is to establish the high pass corner to meet our requirement, as shown in Fig 2. Also, the capacitive feedback is important to block the DC offset, while the resistive feedback is crucial to avoid the input of OTA from becoming a floating point. The closed loop gain is equal to the ratio of the input capacitance(C_{in}) to the negative feedback capacitance with the pseudo resistor (C_{nf} & psdo1). The positive feedback loop (C_{pf}) is mainly is used for increasing the input capacitance. Fig 3. presents the structure of the OTA inside LNA. We use 2 stage differential op amp to achieve high output swing and low noise. The low pass corner is related to the OTA also.

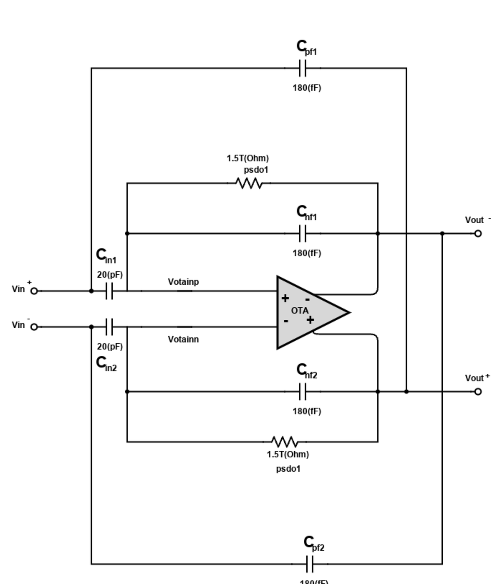

Fig 2. The structure of LNA

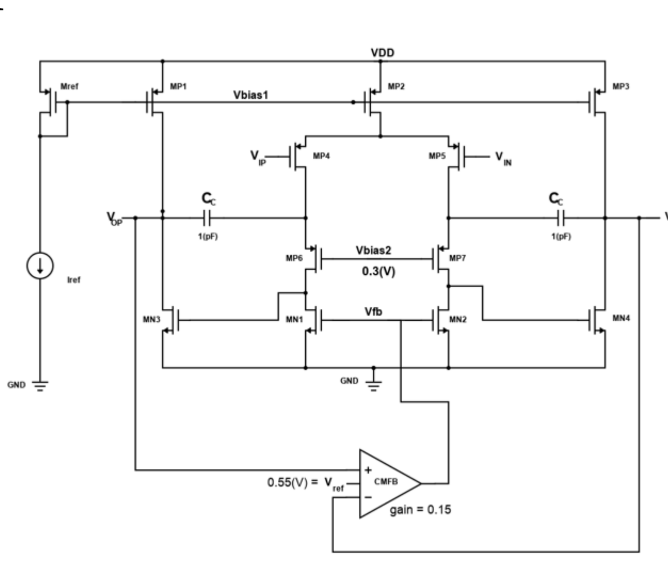

Fig 3. The structure of OTA inside LNA

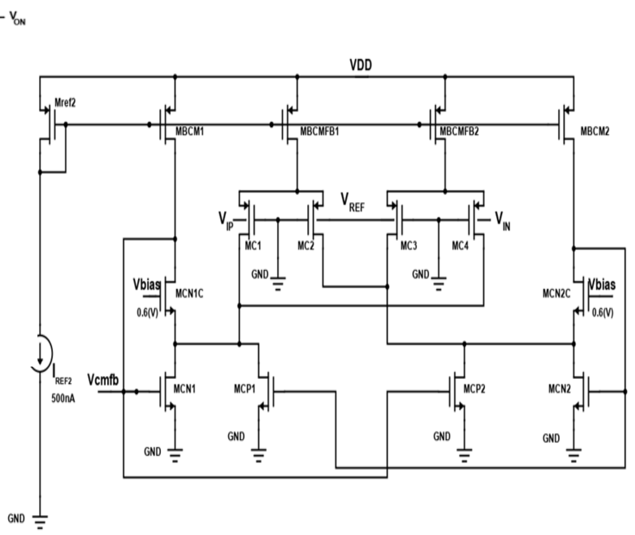

Fig 4. The structure of bulk input CMFB

Fig 4. illustrates the bulk input structure of CMFB. This design is chosen for its low gain and high input impedance, so that it won't affect the stability of the LNA. Fig 5. shows the structure of the V/I converter. This block converts the signal from voltage domain to current domain. The transconductance of the V/I converter relates to the pseudo resistor placed across its two terminals. The resistance of the pseudo resistor is controlled by the bias across it's drain and gate. Here we fix the bias to be 0.5(V) to get a preferable transconductance. Last but not the least, Fig 6. shows the OTA inside the V/I converter. The rail to rail input helps to improve the input voltage range enabling the V/I converter can sustain the high output swing from the LNA.

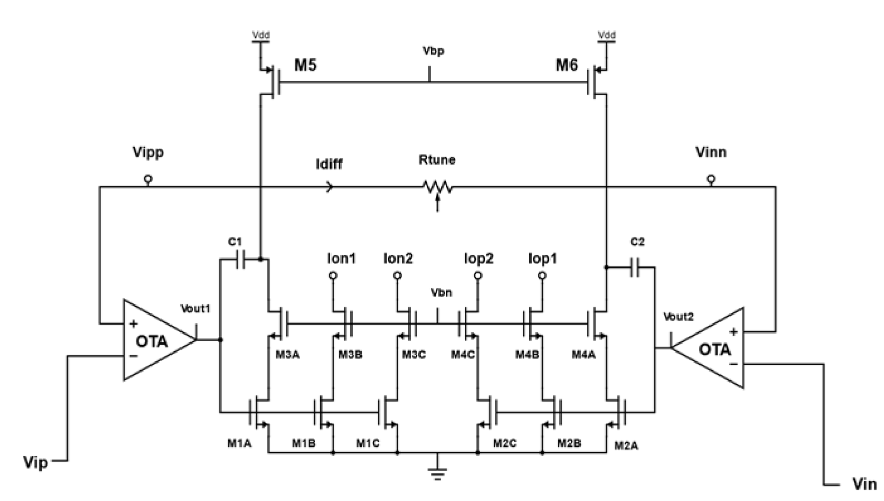

Fig 5. The structure of V/I converter

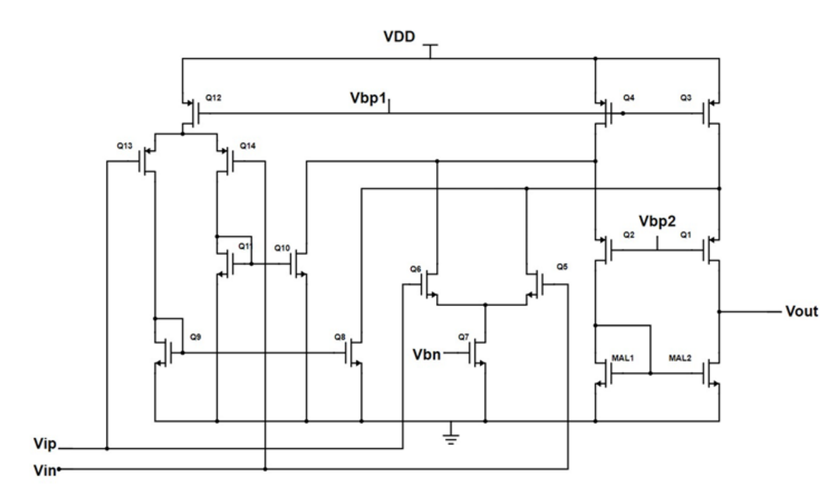

Fig 6. OTA inside V/I converter

Experiment Results

Fig 7. presents the bandwidth and gain information from the pre-simulation results, while Fig 8. shows the results from post-simulation. Besides, Fig 9. illustrates the maximum input and output swing of the V/I converter. A comparison of the overall results with those from reference [2] is provided in Table 1.

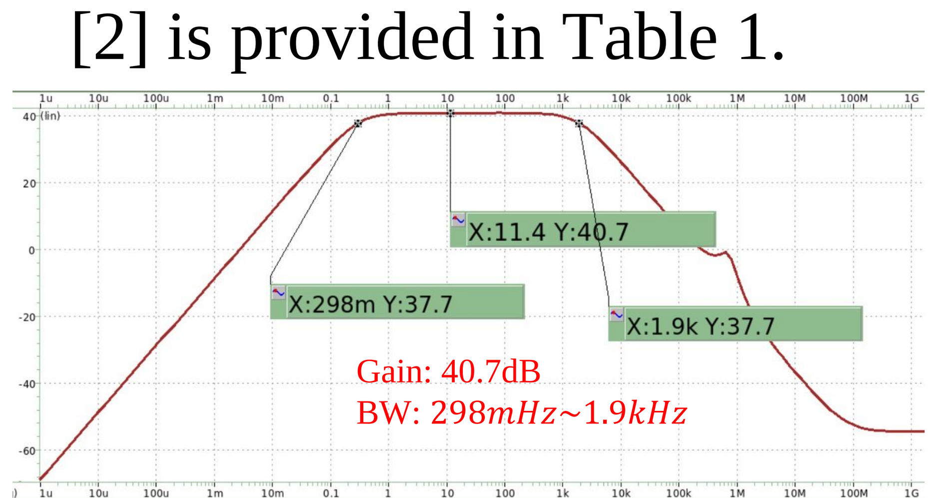

Fig 7. LNA TT pre-simulation result

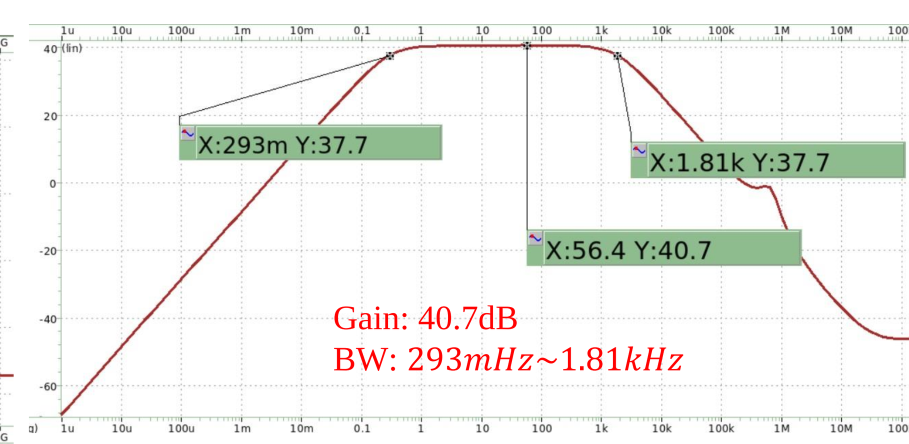

Fig 8. LNA TT post-simulation result

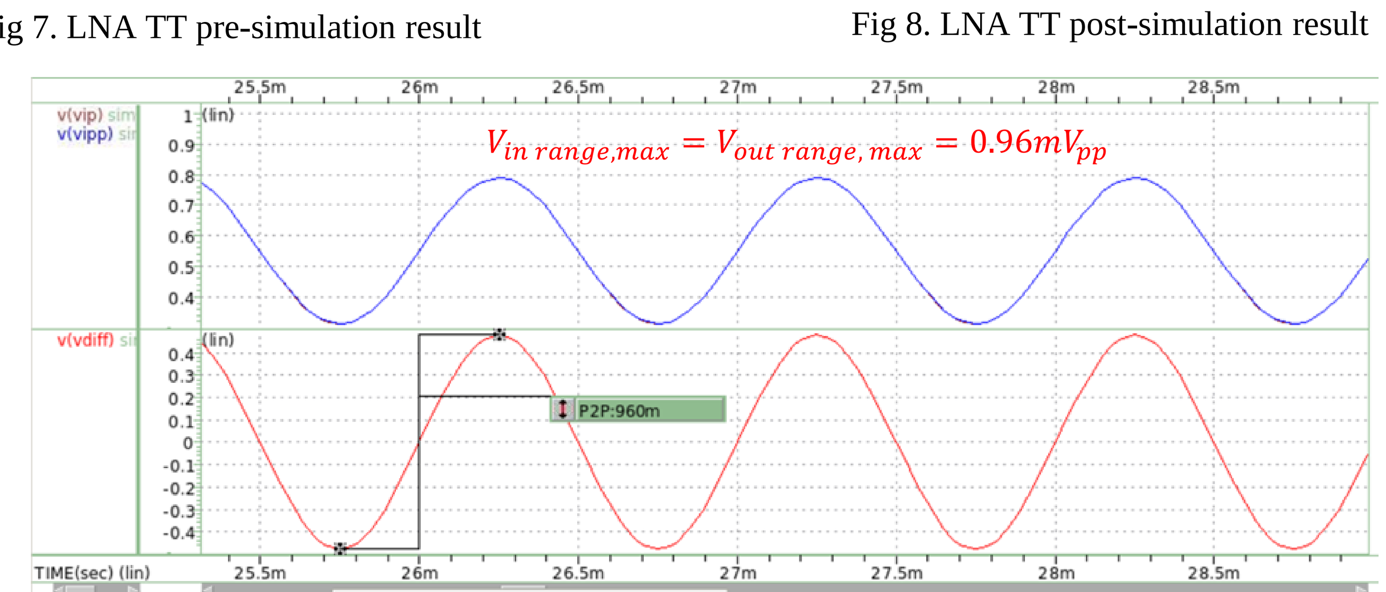

Fig 9. The maximum input and output swing of V/I converter

TT 25°C	spec	Pre-sim	Post-sim	Reference [2]
Input Voltage range	$> 8mV_{pp}$	$9.4mV_{pp}$	$9.2mV_{pp}$	$8mV_{pp}$
LNA bandwidth	$500mHz$~$1kHz$	$298mHz$~$1.9kHz$	$293mHz$~$1.81kHz$	$60mHz$~$0.95kHz$
LNA DC gain	$40dB$	$40.7dB$	$40.7dB$	$34dB$
OTA CMRR (LNA)	$> 90dB@50Hz$	$187.4dB$ @$50Hz$	$173dB$ @$50Hz$	$67dB$ @$50Hz$
Bandwidth in V/I converter	$> 1kHz$	$0Hz$~$1.24kHz$	$0Hz$ ~$1.23kHz$	----------------------------
Input refer noise	$< 37.7\mu V_{rms}$	$29.67\mu V_{rms}$	$31.14\mu V_{rms}$	$3.77\mu V_{rms}$
Voltage supply	1(V)	1(V)	1(V)	1(V)
Power consumption	$< 10\mu W$	$7.2913\mu W$	$8.0952\mu W$	----------------------------

Table 1. the overall experiment result in TT corner 25°C

Reference

•[1] S. S. Udupa, P. S. Sushma and Chaithra, "ECG analog front-end in 180 nm CMOS technology," 2017 International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT), Kerala, India, 2017, pp. 327-330, doi: 10.1109/ICICICT1.2017.8342583.
•[2] Y. Li, A. L. Mansano, Y. Yuan, D. Zhao and W. A. Serdijn, "An ECG Recording Front-End With Continuous-Time Level-Crossing Sampling," in IEEE Transactions on Biomedical Circuits and Systems, vol. 8, no. 5, pp. 626-635, Oct. 2014, doi: 10.1109/TBCAS.2014.2359183.
•[3] LOW-VOLTAGE RAIL-TO-RAIL BULK-DRIVEN CMFB NETWORK WITH IMPROVED GAIN AND BANDWIDTH by Fernando Castafio(J) , Guido ToreU12) , Raquel Perez-Aloi J) , and Juan M Carrillo(l)