Electrical Transport Properties of the Spin Qubit Device

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Abstract

Solid-state qubits, based on electron and hole spins in semiconductor quantum dots (QDs), present a scalable quantum computing platform. Achieving fault-tolerant quantum computing may require millions of physical qubits, making scalability essential. Silicon quantum dots, leveraging microelectronics, offer a promising path toward large-scale quantum systems.

This research focuses on methods for measuring and analyzing spin qubit devices, particularly ambipolar quantum dots in silicon-on-insulator nanowires. Ambipolar devices, capable of operating in both electron and hole modes, provide a versatile platform to combine the advantages of electron and hole spin qubits within the same crystalline environment.

Research Methods and Procedure

This research collaborate with Prof. 陳正中's laboratory in the Department of Physics and Prof. 徐碩鴻's laboratory in the Department of Electrical Engineering in National Tsing-Hua University. The device is provided by SemiQon.

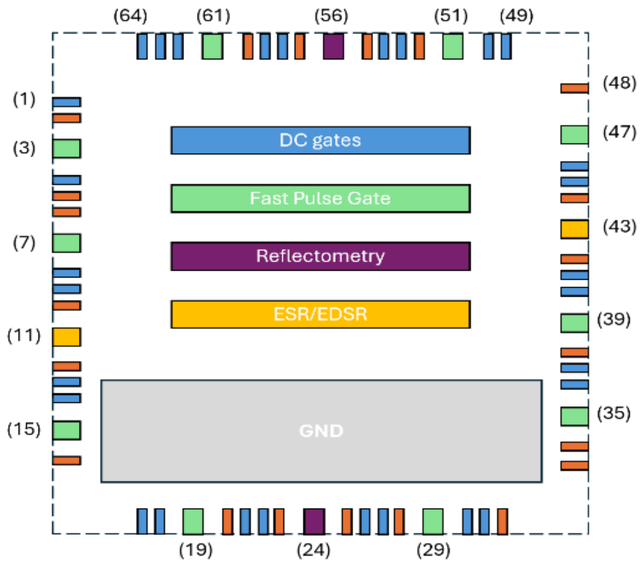
Characterize for electrical leakage between the electrodes. Illustrated by the following device shown on the right. Using the measurement instruments from Wentworth Laboratories and the Agilent B1500A Semiconductor Device Analyzer to determine if there is a leakage based on the obtained current-voltage ($I-V$) curve.

Wire bonding the devices and PCB board. This section delves into the incorporation of electronic components within the printed circuit board (PCB) that serves as a chip carrier for high frequency operations.

Measurements of component characteristics. At temperatures of 4K and below (e.g. 100mK, etc.), various measurements could be performed in this cryogenic system.

Experiment Setup

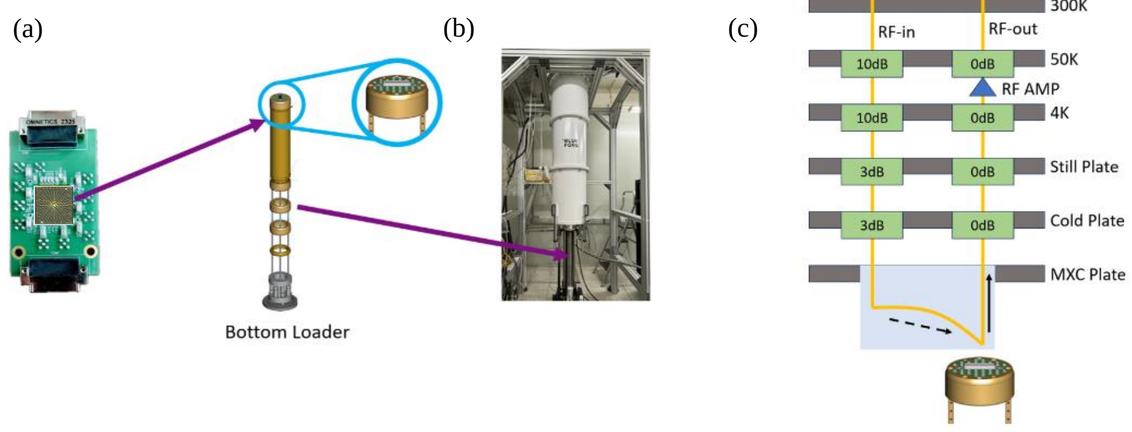
- **Bonding Plan**



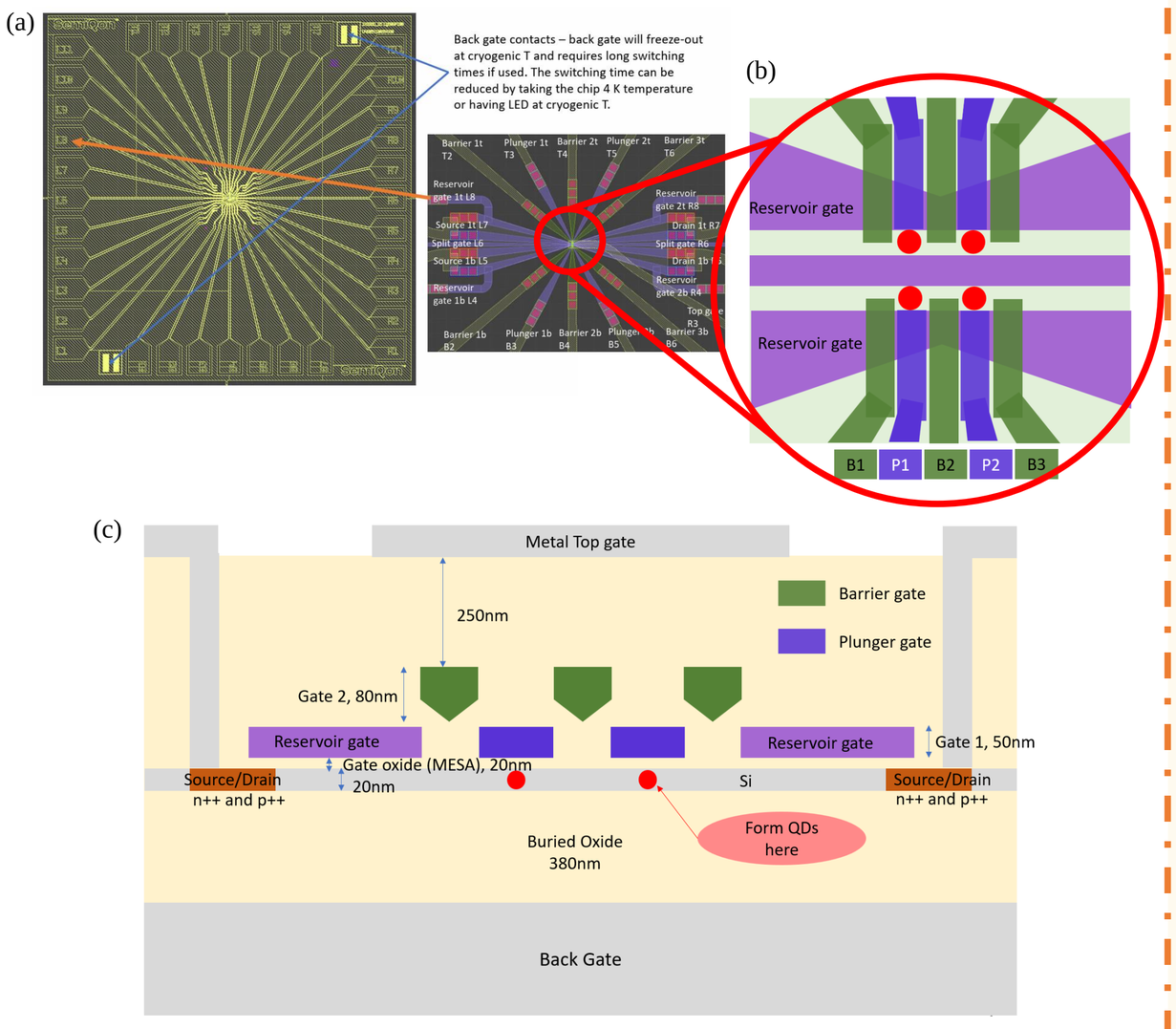
PAD	Gate	PAD	Gate
4	L6	37	R6
8	L5	40	R7
9	L4	41	R8
11	B4	49	T6
17	B2	50	T5
18	B3	51	T4
21	B5	53	T3
22	B6	54	T2
24	R5	56	L7
31	R3	59	L8
36	R4		

- **Low Temperature Measurement**

(a) (b) (c)

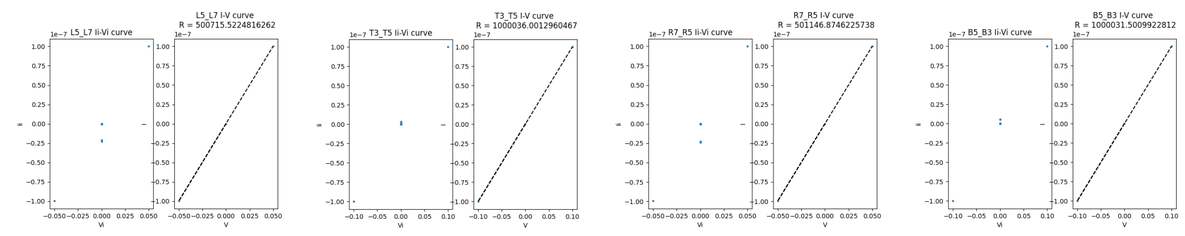


Device Structure

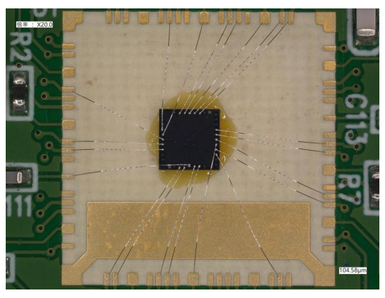


Results

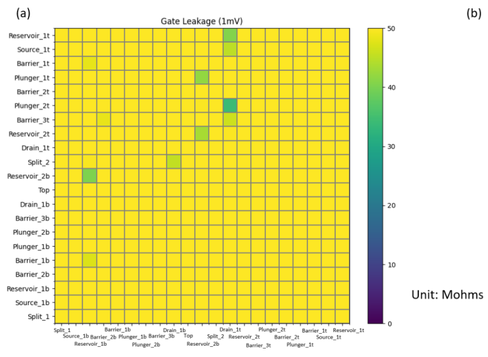
- **Electrical Leakage Between L5-L7, T3-T5, R7-R5, B5-B3**



- **Bounded Device**



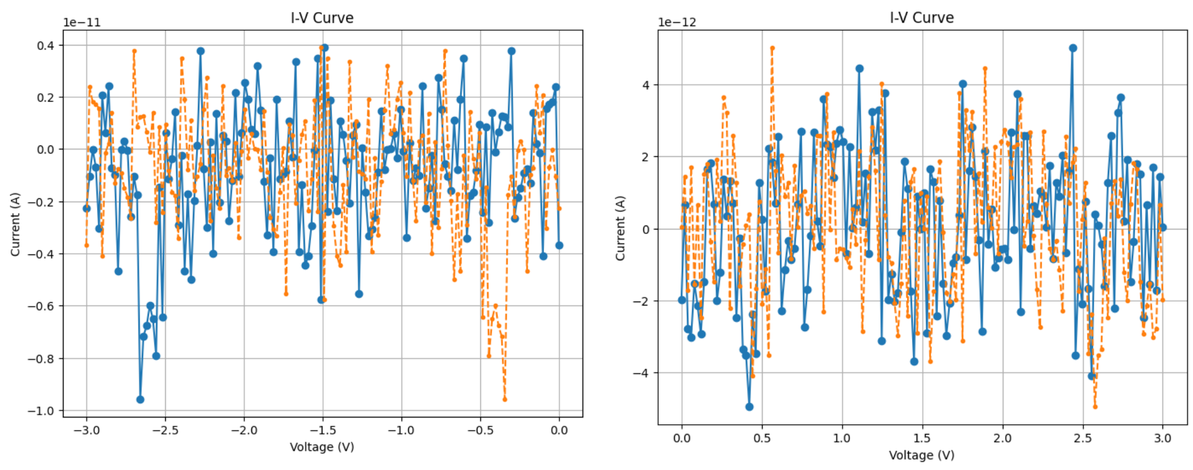
- **Low Temp. (37mK) Gate Leakage Test**



(b)

PCB-PAD	Chip-Gate	
24	L7	Source 1t
27	L5	Source 1b
59	R7	Drain 1t
56	R5	Drain 1b
53	R3	Top
62	R8	Reservoir 2t
58	R6	Split
54	R4	Reservoir 2b
22	L8	Reservoir 1t
26	L6	Split
39	L4	Reservoir 1b
13	T2	B 1t
9	T3	P 1t
8	T4	B 2t
4	T5	P 2t
1	T6	B 3t
37	B2	B 1b
40	B3	P 1b
41	B4	B 2b
45	B5	P 2b
46	B6	B 3b

- **Low Temp. (37mK) Turn on Curve Test of Upper and Lower Channels**



P-type, $V_{SD} = -0.5V$, $V_{top\ gate} = -10V$

N-type, $V_{SD} = 0.5V$, $V_{top\ gate} = 10V$

Conclusion

We measured both upper and lower channel of the device for both N-type and P-type operation, but no turn-on curve was observed even with a $500\ mV$ source-drain bias, leading us to conclude that the device likely suffers from carrier freezing, a common issue that can vary between devices and wafer batches. It is also possible that poor process quality is to blame. The thin silicon channel makes uniform doping difficult, resulting in non-uniform 2DEG or 2DHG formation. Additionally, it is possible that this device is not a degenerate semiconductor.