Department of Electrical Engineering, National Tsing Hua University
Special Topic on Implementation Research Summary

CMOS Heterogeneous Integration using Silicon n-FinFET and 2D WSe_2 p-FET

矽 n-FinFET 與二維 WSe_2 p-FET 的 CMOS 異質整合技術

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Group Number: B427

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Abstract

Two-dimensional (2D) semiconductors for nanotransistor applications have become one of the most sought-after research topics due to their extraordinary properties as the rule of silicon miniaturization journey, Moore's Law, is being close to the end. 2D semiconductors with atomic thickness provide great benefits, such as superior carrier mobility and gate-control capabilities, which help to break the limitations on device scaling. 2D transitional metal dichalcogenide (TMD) materials, such as WSe_2, are both fundamentally and technologically appealing. Because of its sizable bandgap, dangling-bond-free surface, and stability under ambient conditions, WSe_2 is a great candidate for electrical applications, such as the p-FET (P-channel field effect transistor) component in complementary metal-oxide-semiconductor (CMOS).

This project focuses on implementing heterogeneous integration (HI) in p-FET and the stacking process of the CMOS to fabricate an inverter. First, we evaluate the quality and layer quantity of WSe_2 before transferring it to the target substrate. Moreover, select an appropriate contact metal and dielectric oxide to achieve high-performance p-FET. Lastly, connect the p-FET with the n-FinFET that was previously manufactured and verify the functionality of the CMOS. The brief process mentioned above is shown in **Fig. 1**. In this study, we examine the advancements in 2D field-effect transistors for integrated circuits (ICs), focusing on high-density integration, low power consumption, and their significance in influencing the next generation of technology.

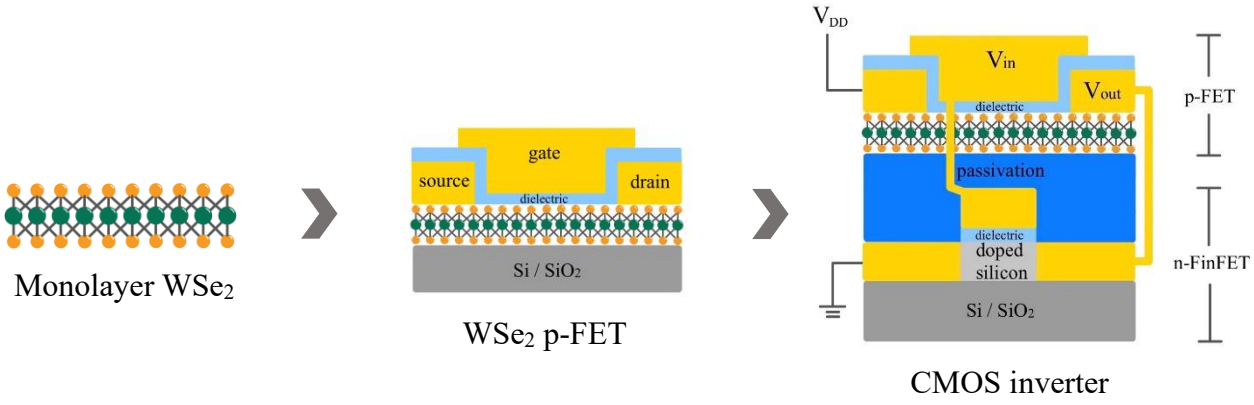

Fig. 1: Schematic experimental fabrication process of HI CMOS inverter

Contents

I. Motivation and Problems

Heterogeneous Integration (HI) technology is an interdisciplinary field of study that aims to connect two different materials and optimize the characteristics of the combination to the maximum extent possible. Researchers have been focusing on this technology (HI) since the 1970s and expect that by the year 2030, it will meet the demand for computing technologies **[1]**. Opting for 2D FET (Field-Effect Transistor) is a brilliant approach to enhance the efficiency of proposed devices. There are a few main reasons:

1. For traditional 3D (three-dimensional) semiconducting materials, some defects and dangling bonds cause bumpy surfaces, which leads to the scattering of charge carriers, resulting in a significant degradation of mobility.
2. A commonly used 3D semiconductor is silicon. One of the reasons for this is that native silicon oxide forms very quickly on the surface of silicon under normal temperature and pressure (NTP), creating an excellent and natural interface between the silicon oxide and silicon. However, the native silicon oxide is too thick, approximately 5 nanometers above the surface of the silicon. Therefore, the silicon thickness thinning down is a big challenge for device scaling.
3. To sustain Moore's Law going further, 3D stacking is a great way to reduce the total footprint required in integrated circuits (ICs). Compact and superior monolithic integration can improve energy efficiency by reducing R-C delay and enhancing signal transport rate.

2D semiconducting materials can solve this problem with their small thickness, resulting in less mobility degradation, suppressing short channel effect (SCE), easier integration, improved efficiency, and better control of the electric field. One of the main goals of enhancing electronic devices is to address the steady energy consumption in integrated circuits (ICs). Typically, inverter building block is a necessary and vital logic gate in ICs, and it can be constructed by an n-type Metal Oxide Semiconductor Field Effect Transistor (NMOS) and a p-type Metal Oxide Semiconductor Field Effect Transistor (PMOS). One of the advantages of CMOS inverter is that it only turns on one MOS at a time, reducing a significant amount of steady energy consumption. For stacking CMOS, the metal is positioned on a 2D semiconductor in a top-gated FET. When combining metal and semiconductor surfaces, the

interface between them can have undesired effects such as Fermi level pinning (FLP). Fermi-level pinning occurs due to the presence of interface states or defects near the interface between a semiconductor and a metal or insulator. These states trap charge carriers, causing the Fermi level to align with them and preventing the carriers from moving freely in response to changes in the material's doping or work function. This phenomenon restricts the control of the Fermi level by external factors, leading to Fermi level pinning. [2] FLP may lead to high contact resistance (Rc), which is difficult to control and can lower the device's energy efficiency. High-κ (high-kappa) dielectric materials are a superior choice to silicon dioxide for the gate oxide material to meet the demands for transistor scaling. High-κ dielectric is a type of material with a high dielectric constant (κ, kappa) compared to silicon dioxide. Advantages of choosing high-κ materials include increased gate capacitance and reduced leakage due to their high dielectric constant and available thin thickness (< 2nm).

This project aims to improve electrical performance of 2D p-FET. It involves selecting dielectrics with moderate permittivity to enhance the gate controllability of the device and demonstrating the results of the inverter to validate the quality of Heterogeneous Integration (HI).

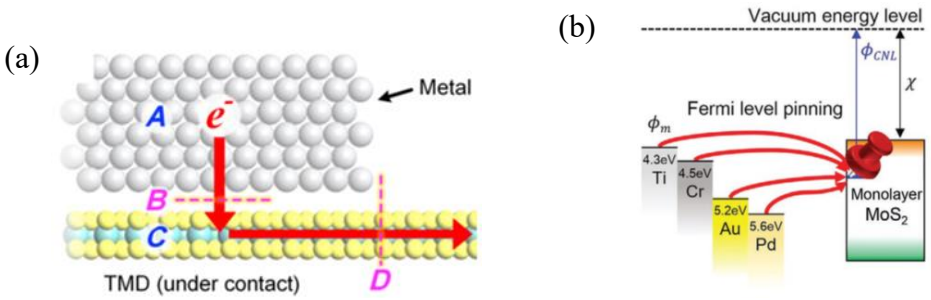

Fig. 2: (a) Cross-sectional view of electron flows through 2D/metal materials contact. (b) Schematic of FLP in monolayer MoS_2. The Fermi level is pinned at the interface of the metal and semiconductor (marked as interface B in picture (a)) [3]

II. Literature Review

2.1 Synthesis of 2D WSe_2

The commonly used methods for the development of 2D materials include mechanical exfoliation, liquid-phase exfoliation, chemical vapor deposition (CVD), and physical vapor deposition (PVD). [4] For WSe_2, the mechanical exfoliation technique (known as the scotch

tape method) has been utilized. Nanosheets produced by mechanical exfoliation exhibit pristine, clean, and high-quality structures, making them suitable materials for studying their inherent thickness-dependent properties. [5] However, to achieve mass production and ensure its quality, it is not a good choice. To produce a single layer 2D WSe_2 using the mechanical exfoliation technique, controlling the thickness and number of layers of the film may incur significant costs. Therefore, we chose CVD in this project. Using the CVD method, multilayer thin transition metal dichalcogenides (TMDs) can be developed over large areas, making them suitable for device applications. [4][6]

2.2 Characteristics of 2D WSe_2

In this project, we chose WSe_2 as the channel material for a 2D p-FET in conjunction with silicon n-FinFET. WSe_2 is a type of transition-metal dichalcogenides (TMDs or TMDCs) with the molecular formula MX_2, where M represents a transition-metal atom (Mo, W, Ti, Zr, Ta, Nb, etc.) and X represents a chalcogen atom (S, Se, Te, etc.). The structure of transition metal dichalcogenide (TMD) monolayers consists of metal atoms interleaved between chalcogen atoms as shown in **Fig. 3**. [7]

2D WSe_2 has many unique properties. When the thickness of WSe_2 is reduced to a monolayer (< 1 nm), there is little to no effect on mobility degradation compared to bulk WSe_2. [8] In its monolayer configuration, WSe_2 has a slightly smaller band gap (~1.65 eV) compared to monolayer MoS_2 (1.8 eV), which has drawn significant attention among various transition metal dichalcogenides (TMDCs). And their bulk forms have a similar band gap of 1.2 eV. Notably, the transport properties of mechanically exfoliated monolayer WSe_2 can be easily tuned to exhibit either p-type or ambipolar behavior, depending on the choice of contact metals. [9]

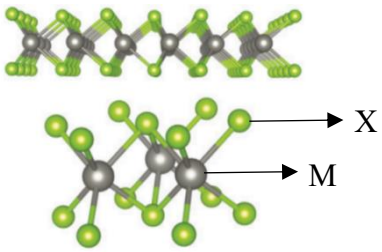

Fig. 3: Structure of monolayer TMDs [11]

2.3 Characteristics of 2D PMOS

The performance of 2D PMOS devices is assessed through electrical measurements, extracting vital parameters such as on-state current per micrometer of channel width (W), on-off ratio, subthreshold swing (SS), contact resistance, and carrier mobility. Notably, a device with a 400 nm channel length exhibits an impressive on-state current of approximately 97 μA/μm, indicative of its high performance. Moreover, its subthreshold swing measures around 140 mV/dec, highlighting favorable device characteristics. Through the transfer length method (TLM), analysis of contact resistance reveals values as low as ~ 6 kΩ-μm, rivaling or surpassing previous records, suggesting robust metal-semiconductor interfaces. Additionally, hole mobility, extracted from resistance versus channel length plots, ranges from approximately 125 to ~150 cm^2/V-s, indicating efficient movement of charge carriers within the channel. These findings highlight the excellent performance of 2D WSe_2 PMOS FETs, demonstrating significant progress in the field of semiconductor technology.

2.4 Structure and Characteristics of CMOS

The goal of this project is to build a CMOS, which consists of a p-FET stack on the n-FET with passivation in between. By connecting the outer connection, the p and n FET will form an inverter. The relationship between the input voltage and the output voltage should be illustrated like which is shown in **Fig. 4**. The blue part represents the passivation layer. The section above is the p-FET, while another half below is the n-FET. The final goal is to vertically stack active devices, such as transistors and diodes, to achieve the ultimate Monotholic-3D (M3D) Integration. This will enable the creation of ultra-high-density M3D-ICs with ultimate thinness for next-generation electronics. **[10]**

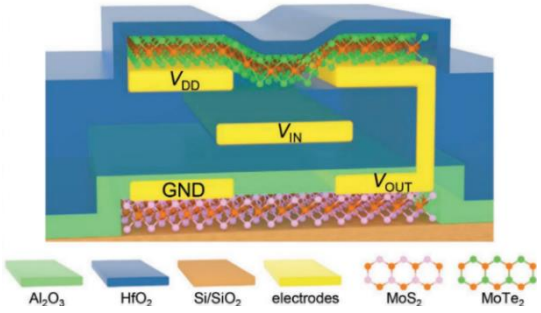

Fig. 4: Schematic Structure of CMOS Inverter **[12]**

III. Methods and Procedures

The main goal of the project is to address the contact issue in the p-FET by integrating it with a silicon n-FinFET, resulting in a CMOS with the characteristics of an inverter.

3.1 Fabrication of p-FET

During the CVD process, the WSe_2 layer has grown on the sapphire substrate. Check the material under an electron microscope to roughly confirm its quality. Analyze it using Photoluminescence (PL) spectra and Raman spectra to determine the number of layers and assess its quality accurately.

A. Transfer of WSe_2 film

The WSe_2 film would be spin-coated with a polycarbonate (PC) layer first, and then the whole substrate (with layers arranged from top to bottom as PC/WSe_2/sapphire) would be immersed in deionized water (DI water). With the assistance of the hydrophobicity of the PC film, WSe_2 can be detached from the sapphire substrate and float up to the surface of deionized water. Then, we place a SiO_2/Si substrate in water and carefully transfer the WSe_2 thin film onto the substrate. The PC should be washed out by chloroform, and the Raman spectra of the WSe_2 should be rechecked to evaluate its quality after transfer.

B. Photolithography

We first spin-coated photoresist onto WSe_2, which is on the SiO_2/Si substrate, so the entire region is coated with photoresist. Next, put on the photomask customized with the correct region to be exposed to ultraviolet (UV) rays by the aligner. This step is for defining the region for later on process, and the pattern will be transfer onto the photoresist. The region defined by the exposure of the negative photoresist to UV rays is covered with the negative photoresist, while the areas without exposure are washed out by the developer.

C. Isolation

To define the device channel, isolating the channel to other area of the WSe_2 layer is

an important step. This can prevent leakage current and non-ideal linkage to other devices. The process is carried out using Dual-Layer Patterning (DLP), which defines the channel region and removes unwanted parts by reactive ion etcher (RIE). Comparing to mask alignment, DLP is much faster and easier to manage.

D. Physical vapor deposition and metal lift-off

Physical vapor deposition is a process carried out in a high vacuum environment where metal is vaporized by heating it to high temperatures and then deposited onto the surface of the substrate. The substrate is coated with photoresist in areas where we do not want the metal to define the drain and source. We then dip the substrate into an acetone solution (ACE) to remove any remaining photoresist, causing the metal/photoresist layer to detach from the substrate. The step is called "lift-off" because the metal is being lifted off the substrate. Finally, use isopropanol (IPA) to rinse out ACE.

E. Add on dielectric layer and gate metal

To add a high-κ dielectric, HfO_2, onto the substrate, atomic layer deposition (ALD) is being utilized in this step. ALD can form a film with uniform thickness for every cycle, and the thickness can be controlled very precisely. For the final step in completing the p-FET, the gate metal is deposited using physical vapor deposition (PVD) and then removed using a metal lift-off process, like step **D** mentioned earlier.

F. Measurement of p-FET electrical characteristics

After the Local Top-gate p-FET is finished, we measure the electrical characteristics with Keysight B1500A.

3.2 Construction and examination of CMOS

A. Stacking

After confirming the n-FinFET manufactured by TSRI (Taiwan Semiconductor Research Institute) is satisfactory, it is ready to be integrated with the p-FET. Passivation is added onto the n-FinFET, and then the p-FET is stacked on top of it. The passivation

layer prevents the connection between the n-FinFET and p-FET, ensuring proper functionality of the CMOS. The outer connection of gates and drains will be completed after the stacking process.

B. Measurement of CMOS electrical characteristics

The final step is to verify if the CMOS can function as an inverter, converting high voltage input to low voltage output and vice versa.

IV. Experiment Results

Although our WSe_2 p-FET and Si n-FinFET prototypes are still in development, we analyzed CMOS heterogeneous integration by referencing the study Monolithic 3D Integration Enabled by Si-FinFET/2D-FET Heterostack by Jhe-Ting Hong et al. **[13]**, which I was one of the co-authors. This work demonstrates the advantages of integrating a Si p-FinFET with a 2D MoS_2 n-FET, combining the high current drive of silicon with the superior electrostatic control of 2D materials. The CMOS structure achieved balanced threshold voltages, high ON/OFF current ratios ($>10^5$), and low leakage currents, making it ideal for energy-efficient applications. The vertical stacking approach reduced the device footprint while maintaining thermal budget compatibility for the 2D material. The resulting CMOS inverter showed high gain and excellent noise margins, confirming its suitability for high-performance logic circuits. These findings provide critical insights for optimizing our own WSe_2-based devices, especially considering WSe_2's potential for high mobility in p-type operation.

Electrical properties of CMOS Heterogeneous Integration using Silicon p-FinFET and 2D MoS_2 n-FET

In the I_{DS} vs. V_{GS} characteristics, MoS_2 (n-type) and WSe_2 (p-type) exhibit opposite exponential trends. MoS_2 shows an increasing drain-source current with rising gate voltage, while WSe_2 displays a decreasing current due to their differing charge carriers (electrons in MoS_2 and holes in WSe_2) resulting in complementary electrical behaviors. Since the properties of WSe_2 inverters have not yet been explored, this analysis will focus exclusively on the characteristics of MoS_2 inverters, acknowledging that the properties may differ significantly.

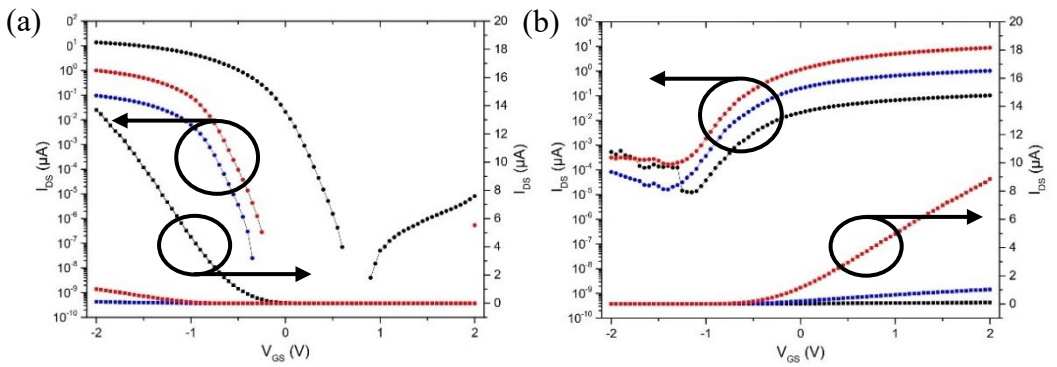

Fig. 5: (a) Transfer characteristics curves of Si FinFETs. The blue and gray lines represent measurements taken before and after the fabrication of the 2D FET on the upper- tier respectively. V_{DS} = 0.01V, 0.1V, and 1V, presented in both log and linear scale. (b) Transfer characteristics curves of top-gate MoS_2 FET. V_{DS} = 0.01V, 0.1V, and 1V, presented in both log and linear scale.

In **Fig. 5**, the transfer characteristics of the Si FinFET and MoS_2 top-gate FET are shown, revealing key insights into the stability and integration potential of these devices. The Si FinFET, as seen in **Fig. 5**(a), maintains consistent performance with negligible degradation after the MoS_2 FET fabrication at different V_{DS} values (0.01V, 0.1V, 1V), suggesting the integration process minimally impacts the lower-tier device. The curves, plotted on both logarithmic and linear scales, highlight the subthreshold region, showing strong on/off ratios and low leakage current. The MoS_2 FET, shown in **Fig. 5**(b), demonstrates high on/off ratios and smooth switching, though its S.S. (204 mV/dec) and V_{TH} suggest room for optimization to align with the Si FinFET's performance for better integration.

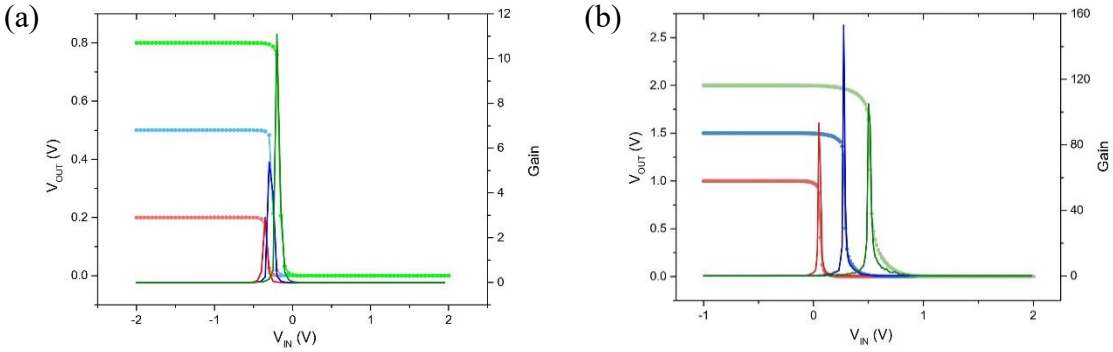

Fig. 6: Voltage transfer curves of the M3D CMOS inverter at (a) V_{DD} = 0.2V, 0.5V, and 0.8V (b) V_{DD} = 1V, 1.5V, and 2V. The darker curves indicate the corresponding voltage gain.

In **Fig. 6**, the gain at higher supply voltages (V_{DD}) is greater, but at V_{DD} = 1.5V, the gain does not follow this trend. This might be due to insufficient data points; this phenomenon can be improved by increasing the point density in the data. Additionally, for a CMOS inverter operating at a supply voltage (V_{DD}) of 1.5V, the calculated noise margins are 0.23V for Noise Margin High (NMH) and 0.38V for Noise Margin Low (NML). These values indicate the circuit's strong resilience to noise fluctuations, ensuring reliable operation in practical applications. These noise margins demonstrate that the inverter can sustain performance across varying conditions, emphasizing the importance of robust design in digital circuits.

V. Conclusions

This project aimed to develop a CMOS inverter through heterogeneous integration, combining 2D WSe_2 p-FETs with Si n-FinFETs. While key processes were successfully optimized—such as the WSe_2 transfer process and the selection of contact metals and dielectrics for p-FET fabrication—the final goal of constructing a functional CMOS inverter was not achieved. This was due to delays in obtaining pre-fabricated Si n-FinFETs and difficulties in synthesizing high-quality WSe_2 via CVD.

Despite these challenges, the project provided valuable insights into integrating 2D materials with silicon devices. Systematic experimentation improved the WSe_2 transfer process and highlighted critical issues, such as material uniformity and contact resistance. The experience also emphasized the need for precise coordination and timing in interdisciplinary projects involving multiple collaborators.

Future work could focus on refining fabrication techniques, ensuring reliable access to pre-fabricated components, and exploring alternative approaches for WSe_2 synthesis and integration. These advancements would address the challenges encountered, paving the way for successful implementation of 2D material-based CMOS technologies in future research.

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VII. Review and Reflections

Technical Achievements and Challenges

This project represents a significant step in my academic journey, allowing me to delve into the intricacies of CMOS heterogeneous integration, an area bridging traditional silicon technology and novel 2D materials. My primary focus was on the fabrication process of 2D WSe_2 p-FETs, which required meticulous attention to detail and a comprehensive understanding of semiconductor mechanisms. Although I successfully completed the fabrication process, challenges arose in ensuring uniformity and optimizing device performance. These difficulties emphasized the importance of precision and consistency in material deposition and patterning.

The collaboration with TSRI provided valuable exposure to advanced device design and fabrication techniques, especially in the development of Si n-FinFETs. While I did not directly contribute to the chemical vapor deposition (CVD) synthesis, integrating these devices into a cohesive framework was an enlightening experience. It underscored the interdisciplinary nature of modern electronics research, where teamwork and expertise from different fields converge to address complex challenges.

Teamwork and Collaboration

One of the most valuable aspects of this project was the collaborative environment. While much of my work was conducted independently, the project as a whole benefited from contributions by TSRI researchers and guidance from Professor Yeh and Jhe-Ting Hong. This collaboration provided me with insights into the design philosophy behind FinFETs and the practical considerations in their fabrication. Communicating effectively with teammates and

understanding their contributions were essential in aligning our individual efforts with the project's goals.

Through this teamwork, I learned to appreciate the diverse expertise required for cutting-edge research. This experience also taught me how to manage dependencies between different components of a project, such as ensuring compatibility between the WSe_2 p-FETs I fabricated and the Si n-FinFETs from TSRI.

Scientific Understanding and Broader Implications

Working on this project deepened my understanding of the physical principles underpinning CMOS devices and heterogeneous integration. The 2D WSe_2 material, with its unique electronic properties, holds immense promise for complementing silicon technology. However, the challenges of interfacing 2D materials with bulk silicon highlighted the need for innovative approaches in contact engineering and thermal management.

Analyzing the results from the referenced study on Si-FinFET/2D-FET heterostacks further reinforced the potential of monolithic 3D integration. The vertical stacking of devices not only reduces the footprint but also enables enhanced performance metrics, such as reduced leakage currents and improved switching speeds. This understanding has motivated me to explore ways to optimize the integration of WSe_2 and silicon devices further, particularly through interface engineering.

Personal Growth and Reflection

This project has been a transformative experience for me, both academically and personally. It challenged me to apply theoretical knowledge to practical problems, bridging the gap between physics and engineering. The hands-on fabrication work was particularly rewarding, as it allowed me to witness the tangible outcomes of my efforts.

I also gained a deeper appreciation for the iterative nature of research. Initial setbacks in fabrication taught me the importance of resilience and adaptability. For instance, when early tests revealed inconsistencies in the WSe_2 layer quality, I refined the fabrication parameters and

improved the outcome. This process of trial and error was a valuable lesson in scientific perseverance.

Future Directions

Reflecting on this experience, I am eager to build on the knowledge and skills gained from this project. One area I am particularly interested in is optimizing the interface between 2D materials and silicon devices to reduce contact resistance and enhance overall device performance. Additionally, I aim to explore the scalability of heterogeneous integration technologies for high-density logic and memory applications.

This project has also inspired me to pursue further studies in advanced nanoelectronics and quantum devices. The integration of 2D materials into traditional electronics represents a paradigm shift in the field, and I am excited to contribute to this emerging area of research.

Conclusion

This project has been a cornerstone in my academic journey, equipping me with practical skills, scientific insights, and a collaborative mindset. It has reinforced my passion for exploring the intersection of physics and engineering, and it has prepared me for future challenges in the field of electronic device research.