國立清華大學電機工程學系：實作專題研究成果報告

Design of a 112Gbps Equalizer in Muller-Muller Phase Detector Receiver for XSR Application in 28nm CMOS

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Abstract

The objective of this research project is to simulate an ideal high-speed serial transmission circuit with a simulation speed set at 56Gbps NRZ (112Gbps PAM4). Based on the simulation results, a practical circuit will be designed to replace the ideal circuit while aiming to achieve similar performance. The impact of different channels (FR4_1p3cm, FR4_2cm, FR4_3cm, FR4_4cm, FR4_5cm) and locking conditions (MMPD) on the SBR (Single-Bit-Response) and the eye diagram characteristics will be analyzed, with a primary focus on the SBR and eye diagram analysis under the MMPD locking condition, that is h-1 = h1. High-speed serial transmission circuits play a crucial role in modern communication systems, making it essential to deeply understand the effects of channel characteristics on signal integrity.

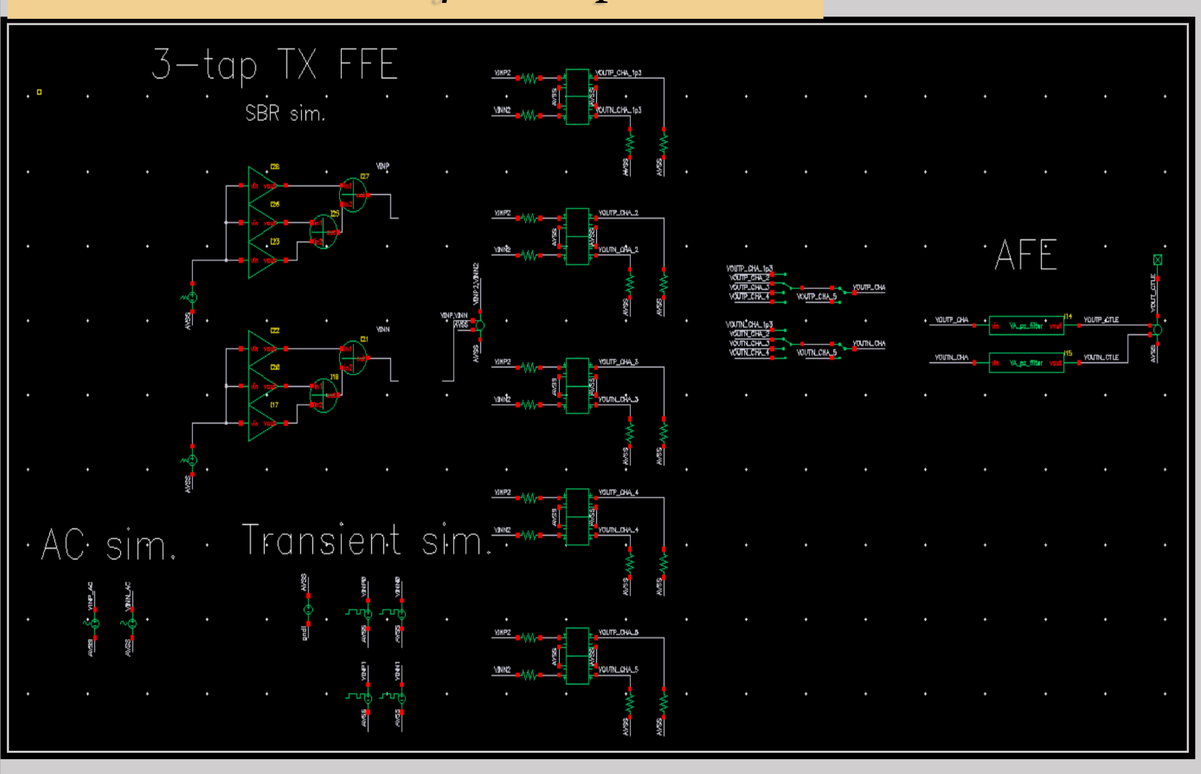
Initially, we designed an ideal high-speed serial transmission circuit, where simulation focused on frequency aspects with modifications made through Cadence IC. Subsequently, simulation software was used to simulate the ideal circuit to obtain optimal performance parameters for the circuit.

Based on the simulation results of the ideal circuit, we designed a practical circuit, considering parameters such as capacitance, resistance, and inductance. Variations in channel materials, lengths, and parasitic effects like parasitic capacitance and resistance were also taken into account. The physical characteristics of the channel have a significant impact on signal transmission speed and quality, requiring adjustments to circuit parameters for optimal circuit performance under different material and length conditions.

The research methodology includes establishing an analog environment, building circuit models, equalizer design, optimizing CTLE (Continuous Time Linear Equalizer), and analyzing SBR and eye diagram graphs. These methods assist in determining the effectiveness of equalizer compensation and evaluating communication quality. In the results section, a series of experimental results were obtained, and equalizers under different channel conditions were optimized to improve the performance of SBR and eye diagram graphs.

In summary, the purpose of this research is to simulate an ideal high-speed serial transmission circuit and design a practical circuit based on the simulation results, aiming to gain an in-depth understanding of the effects of channel characteristics on signal integrity. The research provides valuable reference information to optimize circuit design and ensure high-quality signal transmission.

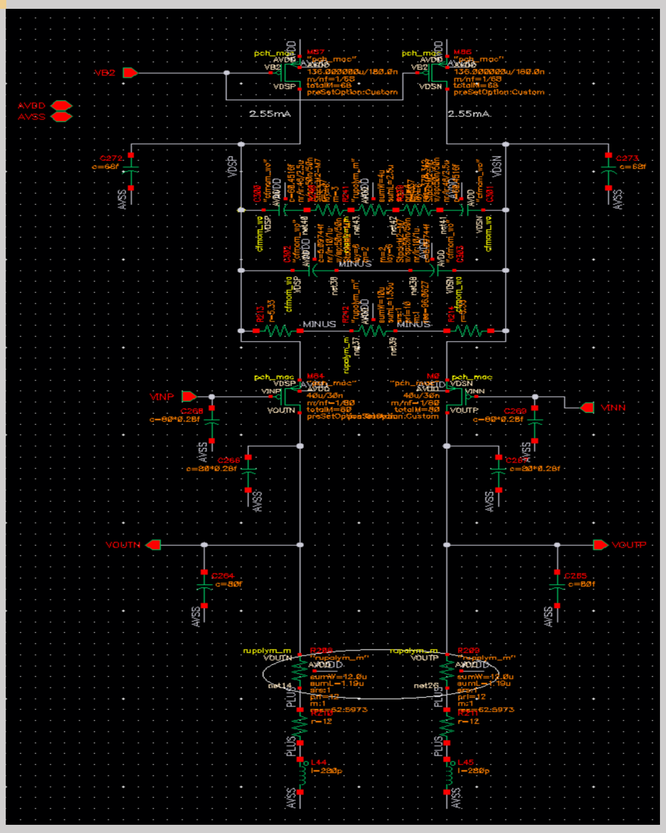
Overall structure of the experiment



(Fig. 1. Schematic of the overall circuit for the experiment)

Research Methodology

We will use software such as Virtuoso Cadence in the laboratory to construct relevant test circuits on the basis of the foundational circuit. Using its built-in ideal pz_filter, we aim to identify an ideal equalizer that corresponds to the AC response and optimizes Single-Bit-Response(SBR) in MMPD locking condition, which also means the cursor points h1 and h-1 in the SBR graph would be the same(h-1=h1). Subsequently, at the schematic level, we will consider parasitic capacitance and parasitic resistance to implement a Continuous-Time Linear Equalizer (CTLE) circuit. Our goal is to achieve an AC response for the practical CTLE circuit that closely approximates the ideal CTLE, thus attaining a similar filtering effect. Finally, we will validate the SBR using this practical CTLE circuit and successfully achieve the desired equalizer performance.

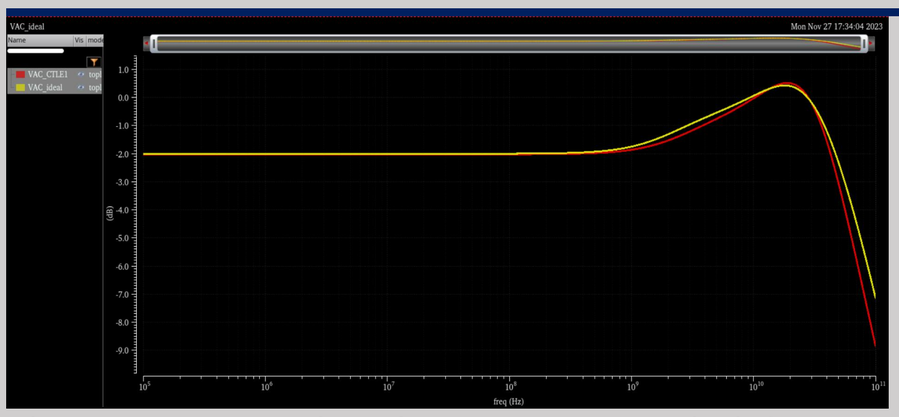


(Fig. 2. The actual CTLE circuit (considering parasitic capacitance and parasitic resistance))

Result & Analysis

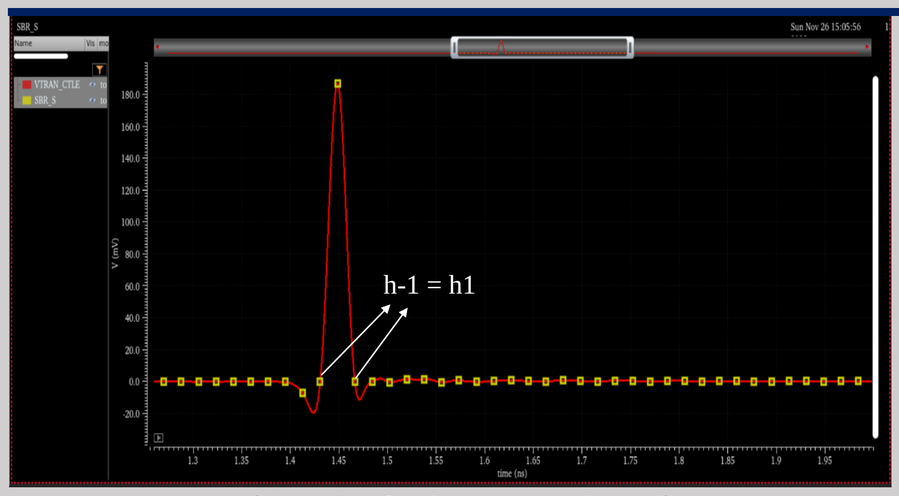
(Fig. 3. Results of the AC response for the FR4_1p3cm to 5cm channel)

Based on the Fig. 3., it can be observed that the channel exhibits a noticeable dB attenuation starting at 28GHz, and the attenuation level increases sequentially from 1.3cm to 5cm, as indicated in Fig. 3.



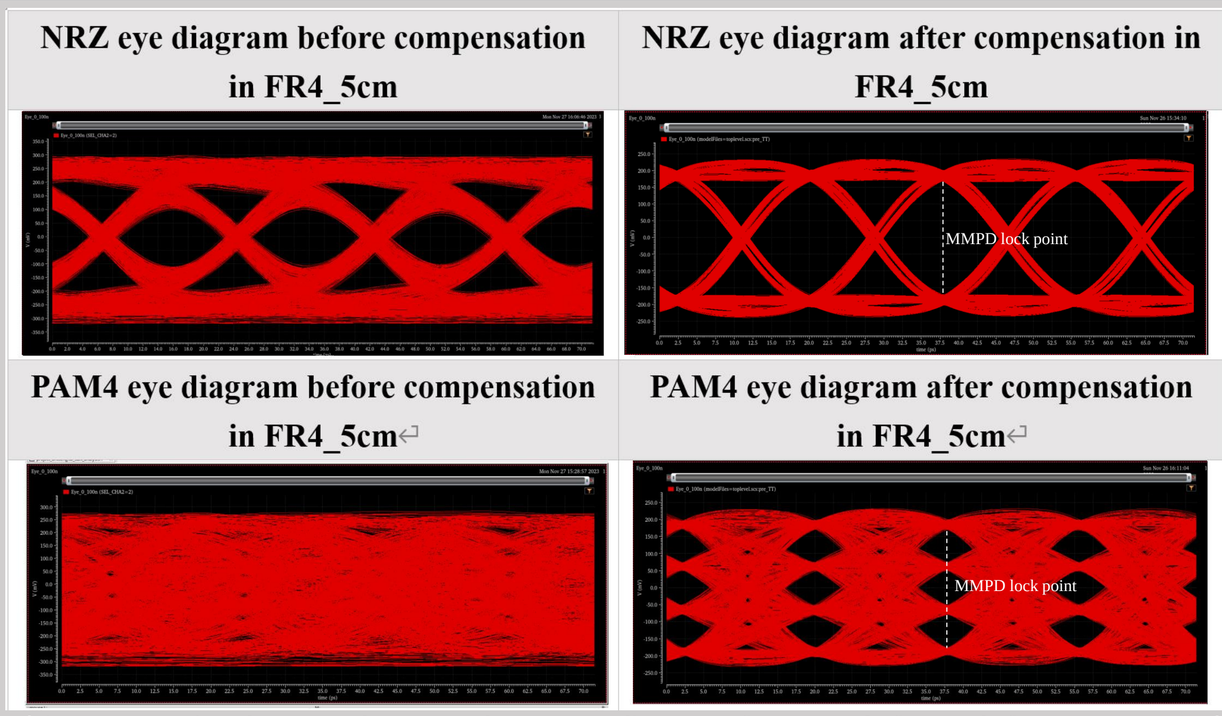
(Fig. 4. Ideal AC response (yellow) and the actual response (red) of the CTLE for the FR4_5cm channel)

In Fig. 4, it can be observed that the implemented CTLE (Continuous-Time Linear Equalizer) exhibits an AC response similar to the ideal CTLE. This indicates that both show similar high-pass filter characteristics.



(Fig. 5. SBR for the FR4_5cm channel)

The cursor points h1 and h-1 below the tip of the SBR graph on both sides are observed to be close to zero (< 2mV) and has the same values (h-1=h1) due to the MMPD locking condition. The SBR graph becomes better, indicating that the implemented CTLE circuit effectively compensates for the signal. This also implies that the CTLE circuit we constructed performs well in its role as an equalizer in signal transmission.



(Fig. 6. Comparison between the NRZ and PAM4 eye diagrams of FR4_5cm before and after compensation)

- The eye diagram in Fig. 6. improves significantly after the application of our equalizer.

Conclusions

In summary, this research project focuses on the critical aspects of high-speed serial transmission circuits in modern communication systems, with a particular emphasis on the profound impact of channel effects on signal integrity. Through the simulation of ideal high-speed serial transmission circuits and the design of practical circuits, we conducted a detailed assessment of the influence of different channel materials and length on the Single-Bit-Response(SBR) plots under various locking conditions. The report provides in-depth analyses of the basic circuit architecture of equalizers, the analysis of Muller-Muller Phase Detector (MMPD) locking conditions, and the effects of different FR4 materials and lengths on the circuit. Comparisons of SBR plots highlight the significant impact of the dielectric height of different channels on signal quality. Throughout the parameter adjustment process, considerations were given to the effects of parasitic capacitance and parasitic resistance. By adjusting parameters such as capacitance, resistance, and inductance to find corresponding poles and zeros, the practical circuit's simulated AC response closely matched the ideal circuit's simulation results.