A Low-Noise Neural Signal Amplifier with Adjustable Gain and Bandwidth for Capturing AP/LFP Signals Separately

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Abstract

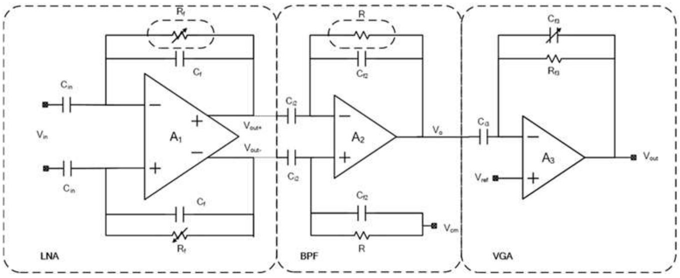
A low noise, low power, neural recording analog front-end (AFE) integrated circuit (IC) is presented. The gain and bandwidth of this work can be changed according to different neural signals. The total gain is between 42.7dB to 47.7dB. With the tunable pseudo-resistor, the low cut-off frequency can be adjusted to 20Hz and 300Hz, and the high cut-off frequency is 4kHz. The achieved input-referred noise is about 7.17μVrms. The total power consumption is 1.60μW with a 1-V supply.

Keywords: Neural Recording Amplifier, Low Noise, Low Power, Tunable Pseudo-Resistor

Background

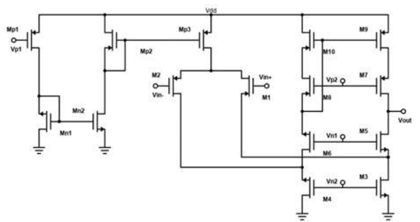
The analog front-end amplifier (AFE) is one of the important blocks in the design of a neural recording system. This block is located after the electrodes and amplifies the received neural signals then processes to other blocks. Neural signals contain frequency components with different ranges and amplitudes.

Implementation

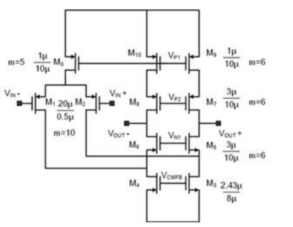


▲ Fig1. Block Diagram of three stage low-noise amplifier.

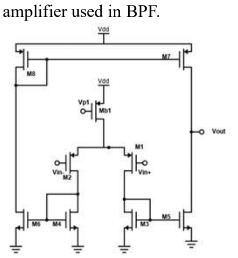
Fig.1 shows the overall structure of the proposed neural recoding analog front-end. This structure consists of three stages. The first stage is a low noise amplifier (LNA) and the second stage is a band-pass filter (BPF). A variable gain amplifier (VGA) is utilized in the last stage. The capacitive-resistive feedback network is used in all three stages, which is possible to block the DC offset generated due to the electromechanical reaction that occurs at the electrode-tissue interface. The voltage gain is equal to the ratio of the input capacitor and feedback capacitors. The voltage-controlled pseudo-resistors are used to change the low cut-off frequency to separate the neural signals with different frequency ranges.



▲ Fig3. The single-ended folded-cascode amplifier used in BPF.

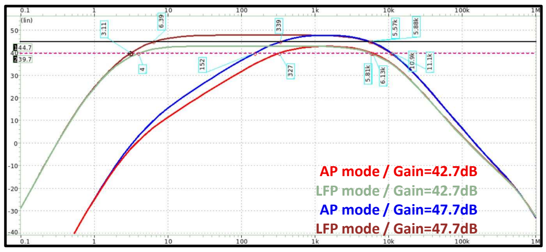


▲ Fig2. The folded-cascode amplifier used in LNA

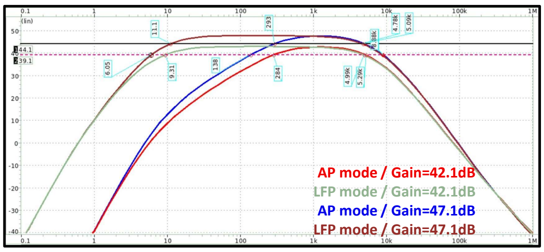


▲ Fig.4 The two-stage amplifier used in VGA

Fig.2 shows the amplifier schematic of LNA. In this work, a fully-differential amplifier is used because the fully differential amplifiers have a high CMRR than single-ended amplifiers. Fig.3 shows the amplifier schematic of BPF. Since the input-referred noise of BPF is divided by the gain of the LNA. Therefore, a single-ended amplifier is used to design the BPF in the second stage to reduce the required power consumption and die area. Fig.4 shows the amplifier schematic of VGA. Using a variable gain amplifier can amplify the neural signals with sufficient gain resulting in enhanced dynamic range in the total system.



▲ Fig5. Simulation result for pre-sim (-3dB pole)



▲ Fig6. Simulation result post-sim(-3dB pole)

TT 37℃	spec	Pre-sim	Post-sim	[1]	[3]
Total current(uA)	-	1.60	1.65	3.60	2.82
Gain(dB) Clk=0/Clk=1	>40	47.7 / 42.9	47.1 / 42.1	45 / 55	45/ 63
Bandwidth(Hz) AP/LFP	20-4k / 400-4k	6.5-5.51k / 335-5.94k	10.8-4.56k / 300-5.09k	0.8-4.15k / 300-8.2k	1-0.5k / 800-5.8k
Power(uW)	<6	1.60	1.65	3.60	2.82
Noise (uVrms)	<15	7.17	8.05	2.1	3.6
Supply voltage (V)	1	1	1	1	1
PSRR(dB) AP/LFP	>60	70 / 67	68 / 67	92.48	70
CMRR(dB) AP/LFP	>60	78/70	66.9/65.1	98.28	80

▲ Table.I. Performance of this work and comparison of amplifier in this work with reference

The test chip is fabricated in TSMC 0.18μm CMOS process, and the chip size is $965\mu m * 965\mu m = 0.93\ mm^2$.

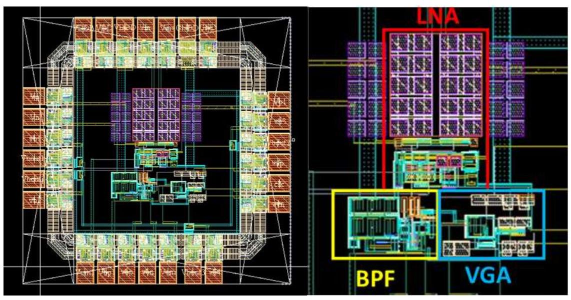


Fig7. Neural recording amplifier layout (T18) ▲

Reference

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