A 6-bit 25MS/s 3-bit/cycle SAR ADC with BDCO

一個六位元每秒取樣二千五百萬次的連續漸進式類比至數位轉換器使用邊界錯誤碼取代機制與每週期比較三位元技術

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Abstract

This work represents a 6 bit 25MS/s 3-bit/cycle SAR ADC with BDCO. This work utilizes the spilt capacitors arrays to reduce the number of capacitors. During the sampling phase, the differential input signals (Vinn and Vinp) are sampled onto the top plate of the DAC capacitors arrays by bootstrapped switch circuit. At the same time, the bottom plate of the DAC capacitors is preset to the given voltage. Then, switching some of the bottom plate of DAC array to precharge the top plate. Due to the interpolation, the DACs and the dynamic pre-amplifiers are reduced from 7 to 4 with only two extra dummy latches. The comparator give their decision at Clkst = 1 to control DACs to switch a successive-approximated residue via the SAR logic, and produce a thermometer code for decoding MSB(3 bits). Next, the precharging operation repeats but switching the DAC arrays bottom plate for the second cycle's reference voltages (1/64−7/64Vref) which is followed by the second comparisons. Each comparison resolves 3 bits resolution and all comparators' outputs are consequently decoded through the decoder to obtain a binary output. For the case the differential input voltage near the reference voltage which is vulnerable to the comparator, we adopt the BDCO(Boundary Detection Code Overriding) circuit. BDCO circuit provide the mapping table to decide the output of 6 bits, which means the result of the second comparison is no longer important.

The simulation SAR ADC uses MOM capacitor structure to deduce the error from capacitors mismatch. The designed SAR ADC is expected in T18 process under 1.2V.

Key word: analog-to-digital converter, successive-approximated, multi-bit/cycle, interpolation

1. Background

Today, analog-to-digital converters (ADCs) are generally classified into three categories: Flash ADC, SAR ADC [1], and Sigma-Delta ADC. In the realm of integrated circuit design, SAR ADCs are known for their lower power consumption but are relatively slower in conversion speed. On the other hand, Flash ADCs maintain the advantage of faster conversion rates, but due to the requirement for numerous comparators, multi-bit Flash ADCs are not conducive to practical implementation.

2. Purpose

The benefits of SAR ADC and Flash ADC are mentioned above. This project focuses on SAR ADC as the core, integrating the strengths of Flash ADC. It adopts a multi-bit conversion mode per cycle and interpolation to enhance the conversion speed of SAR ADC [2][3].

The circuit architecture of this project, as illustrated in Figure 2-1, includes a pre-amplifier processed using interpolation, DAC structure, simplified switching circuit modes, Boundary Detection Code Overriding (BDCO) mechanism, and bootstrapped switches.

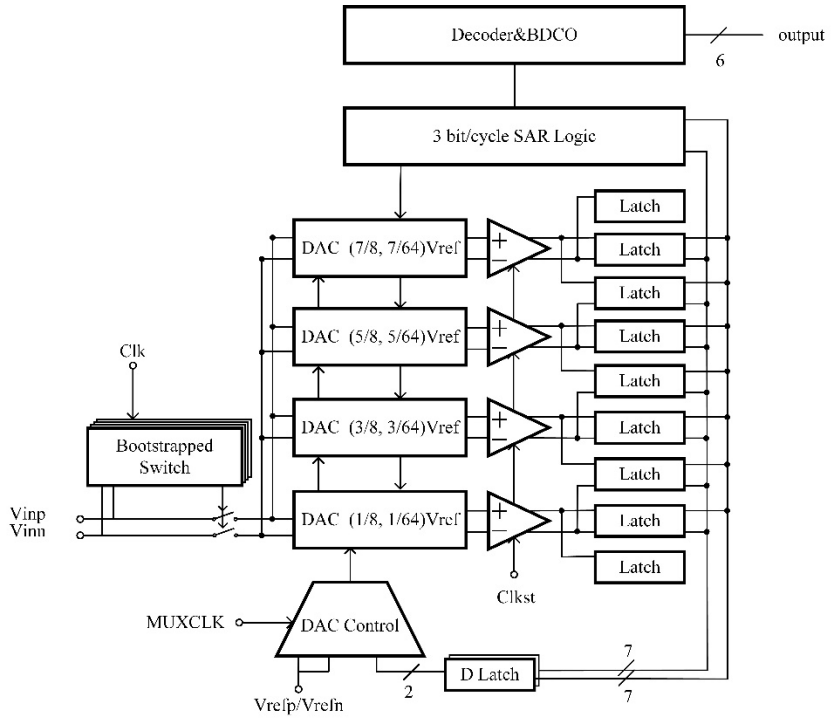

Figure 2- 1 3-bit/cycle SAR ADC with BDCO Architecture

3. Research Method

3.1. Switching Scheme

Fig. 3-1 shows an example of the DAC7 switching scheme with a 7/8 Vref reference voltage. For the first six capacitors during sampling phase (Step 1), three of them are preset to Vrefp and others to Vrefn. In the first precharging phase (Step 2, where the input shift with the corresponding reference voltage), only the capacitor preset to Vrefn is switched to Vrefp while the others remain unchanged in this scheme; therefore, it totally increase 3/8 (Vrefp – Vrefn) on the top-plate of negative terminal of the DAC7. Next (Step 3), the comparators' controls B1-B7 that are in thermometer switch the bottom-plates of the DAC7. If B = 1, the corresponding bottom-plates of the DAC7 will switch to Vrefp and vice versa. The switching scheme on the top-plate of positive terminal of the DAC is complete opposite; therefore, it can make different voltage bound such as ±6/8Vref、±2/8Vref and interpolate on comparator of the second-stage to generate ±4/8Vref、±2/8Vref、0. Fig 3-2. show the voltage change of switching operation. After Step 3 and switch four DACs, we complete first phase to generate 3 bits output codes, and narrow down the comparative voltage range in order to generate the other more precise 3 bits.

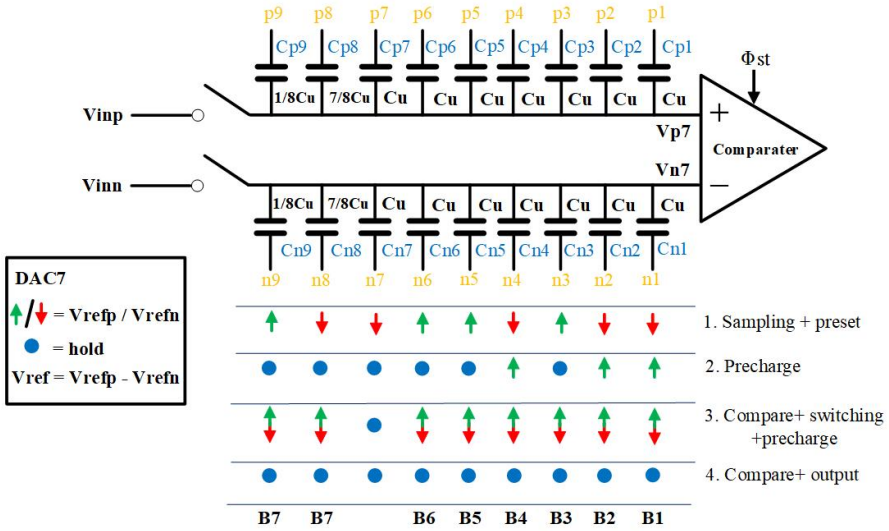

Figure 3-1 DAC7 Switching Scheme

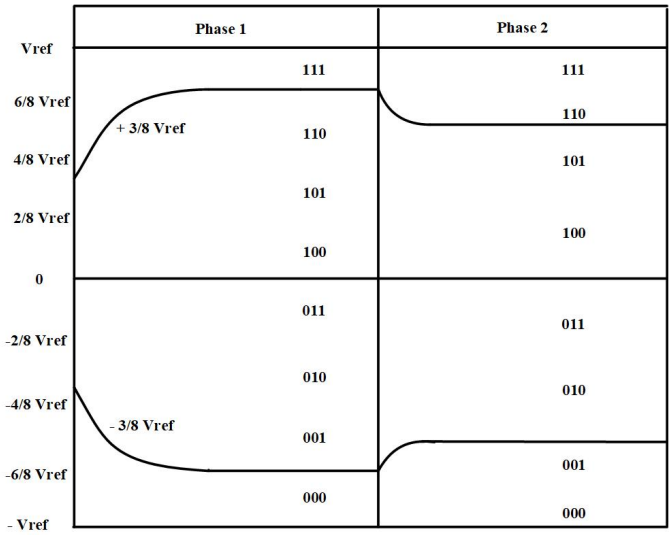

Figure 3-2 Waveform of proposed switching procedure.

3.2. Interpolation

The comparator of our ADC uses interpolation. The output of the pre-amplifier is interpolated to 3 latches, and then the latches will generate 3 required thermometer boundary values: +4/8Vref, 0Vref, -4/8Vref. The advantage of the interpolation structure is to reduce the number of pre-amplifiers. Without interpolation, it would require 7 pre-amplifiers and 7 latches. However, by using this method we only need 2 additional dummy latches, reducing the required number of pre-amplifiers to 4. We use HSpice to simulate the offset of the comparator. By 500 times of Monte-Carlo simulation, we get the average Offset voltage of our comparator is 1.33mV, approximately equals to 0.0739LSB (Our 1LSB = 18mV).

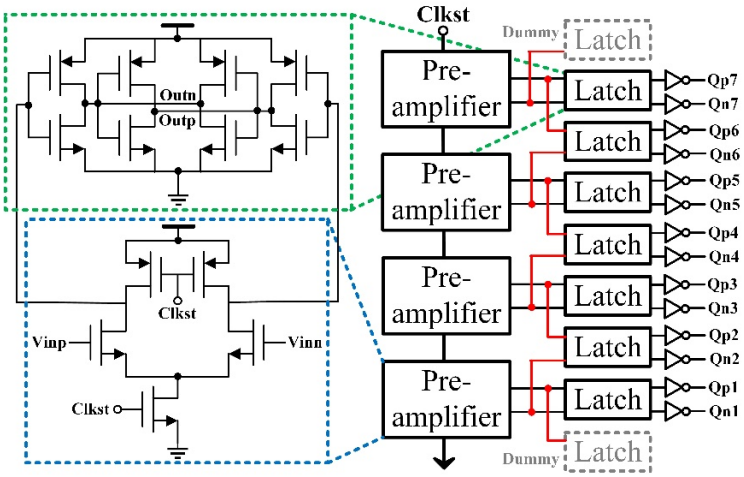

Figure 3-3 Comparator and Interpolation

3.3. BDCO (Boundary Detection Code Overriding)

The BDCO circuit detects whether the comparator encounters input signals with

extremely small differences, which generate a pair of non-differential control signal (Dp, Dn). The architecture is shown in Fig 3-4. It uses 7 simple XNOR gates to check if all seven pairs of Dp, Dn are different. If one of B1 ~ B7 equals to 1, the signal value becomes 1 through an OR gate, and the MSB part of the output (3 bits) is replaced with the corresponding encoding code in the mapping table. Under these conditions, the residue voltage and the result of the second cycle of comparison are no longer crucial and will not be used to decode the LSB part of the output (3 bits). The BDCO mechanism controls the LSB part of the output to be 000. If any of B1 ~ B7 are not detected as 1, ADC will handle all output bits through conventional decoding.

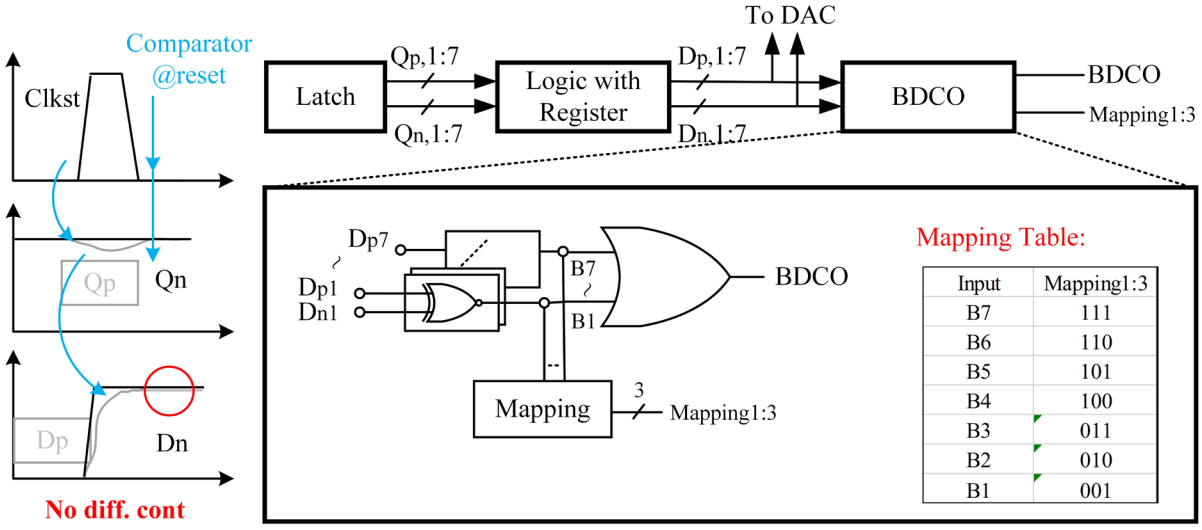

Figure 3-4 BDCO Scheme

4. Experimental Results

Table 4-1

Pre-simulation result under VDD = 1.2V, Sampling rate = 25MS/s

	TT	SS	FF	FS	SF
SNDR(dB)	37.09657	37.17924	36.84520	36.82769	37.05227
ENOB(Bits)	5.869862	5.883594	5.828106	5.825199	5.862503
SFDR(dB)	49.46530	49.96652	48.79998	48.81504	49.54796
Power(mW)	1.2482	1.0483	1.5735	1.1968	1.2637

5. Conclusion

The pre-simulation results in 5 corners are shown in Table 4-1. We have referenced the operational switching modes from [2]. However, in the 180nm process, parasitic capacitance poses challenges, rendering the circuit unable to operate properly. For instance, in the implementation reported in reference [2] using the 65nm process, a single capacitor array requires only 6.4fF, while our single capacitor array needs 128fF to achieve an ENOB of 5.86 or above. This not only prolongs the charging and discharging time of capacitors, affecting circuit performance, but also results in a significantly larger circuit area. Therefore, to pursue higher sampling frequency in this SAR ADC architecture, an advanced process technology is necessary.

6. Reference

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7. 心得

宋姿瑩:

會選擇這個電路實作的專題是因為大三上修了積體電路設計導論以及專題教授所開的類比電路設計一，而被類比電路的魅力深深吸引，在實作 SAR ADC 時，我們遇到很多困難，像是寄生電容造成 DAC 頂板充放電不理想，而使 ADC 不夠準確和比較器在不同的 Corner 下，需要的反應時間不同，可能造成同一筆輸入有不一樣的輸出，從每一次的失敗中找出解法，使我們更了解每一顆 mosfet 在電路中的關係，在電路的實作上，也有明顯的進步。最後，感謝鄭桂忠教授有趣的教學，啟發我對類比電路的興趣，也感謝專題學長犧牲自己的暑假一步步帶領我們完成這令我難忘的電路，在我們遇到難題，進度停滯好幾週時，替我們指點迷津，也感謝同組成員蔡佩諭以及陳立萍，在我遇到困難時即使給予我幫助，一起努力找出解決方法，透過討論交流學習彼此對電路不同的見解，而得到這次的寶貴的實作經驗。

陳立萍:

在大三時我修習了許多類比電路設計類的課程，激發了我想對於類比電路深入研究的好奇心，因此我選擇鄭桂忠教授的 ADC 專題。在大三下專題的第一學期，我們研讀了非常多 ADC 的論文。到了學期中，我們決定好要實作出來的 ADC 架構，並研究其運作切換的演算法。到了6月底開始以 hspice 進行電路建置與模擬。在這個設計過程中我學到了許多電路設計上之必須考量，像是比較器的偏移電壓以及寄生電容之影響；而整個 ADC 的控制訊號必須全面考量到每一個部分的工作時長。謝謝我的隊友佩諭和姿瑩，在遇到問題的時候一起討論解決的辦法。感謝林瑞庭學長與蔡承峻學長每週都會與我們開會討論專題。最後，非常謝謝鄭桂忠教授給予我寶貴的專題研究機會，讓我可以充分了解整個 ADC 從無到有的設計過程。

蔡佩諭:

修完類比一後，我覺得類比電路設計很有趣，因此選擇找鄭桂忠教授製作類比相關專題，而在決定做 ADC 後，我們花了一個學期理解 ADC 的基本操作原理跟找尋有趣的電容切換架構法，並花了許多心力理解論文。猶記第一次看到自舉式開關能完整執行 S/H，內心激動不已；針對 BDCO，參考論文內描述的用途，配合我們實際的架構，將腦中所想實作出來讓我非常開心。我認為真正困難的是將所有電路整合起來，要考量各級電路的推力、時序產生、在不同 corner 下元件的表現……等，也常常需要

考量整體效果而更改裡面的小 block，但最後整合完並測量效能後，我覺得很有成就感！最後謝謝我的隊友立萍跟姿瑩，在我有問題的時侯能夠給予我意見，也謝謝實驗室裡的學長姐們耐心的幫助我們，特別感謝林瑞庭學長跟蔡承峻學長，用他們的專業知識協助我們跨過難關。