A Comparison of Pulse Width Modulation Image Sensor and 3T Active-Pixel Sensor Using Different Readout Technique

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Abstract

In recent years, Complementary Metal-Oxide-Semiconductor (CMOS) image sensors have been widely utilized in fields such as Internet of Things (IoT), healthcare, and artificial intelligence, where the demand for low-power image sensors is critical. Among these, 3T active pixel sensors and Pulse-Width Modulation (PWM) image sensors are commonly used. Therefore, our goal is to implement these two different types of image sensors and evaluate the advantages and limitations of each.

Goal

This project primarily aims to design a PWM image sensor with enhanced linearity that also effectively reduces the impact of process variations. Furthermore, we plan to integrate the traditional high-linearity 3T image sensor and the PWM image sensor into a single chip. This integration will enable a direct comparison of their light-sensing performance and facilitate a comprehensive evaluation of their linearity under different readout methods.

Implementation

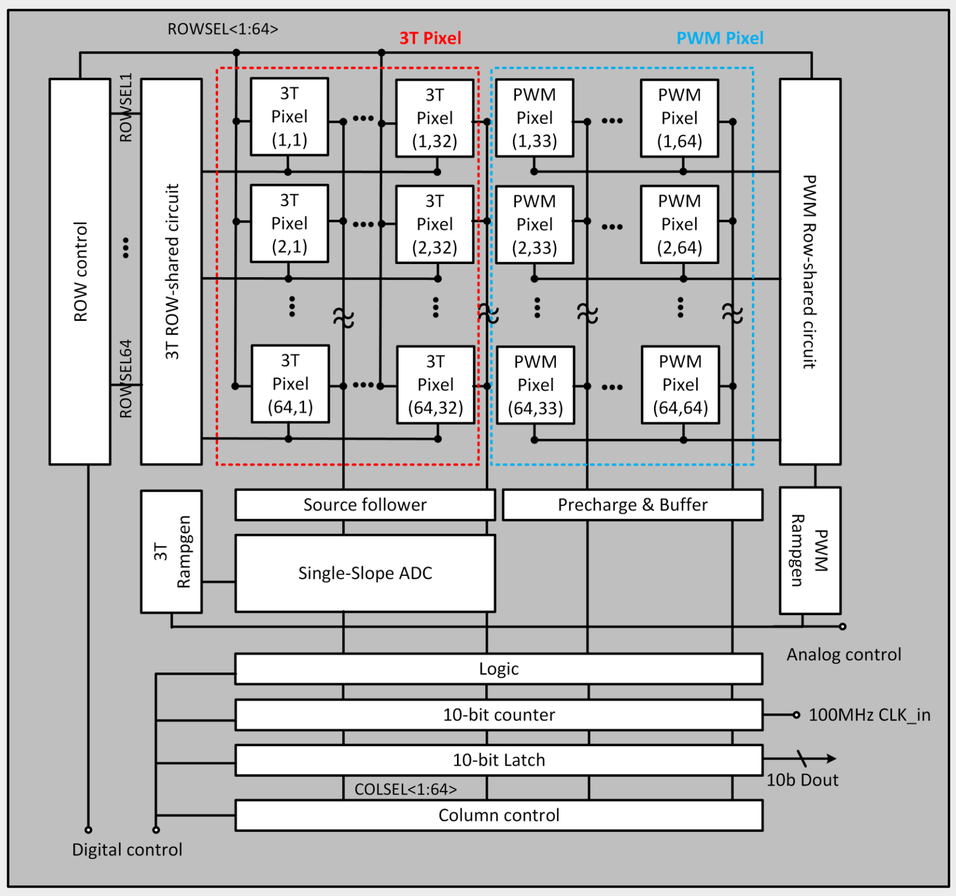


Fig1. System Architecture

As shown in Fig1, this chip is composed of a 64x64 pixel array (including 64x32 3T-pixels and 64x32 PWM-pixels), a 3T/PWM ramp generator, ROW/COLUMN control circuits, 3T/PWM row-shared circuits, 3T/PWM column-shared circuits, logic circuits, a 10-bit counter, and a 10-bit latch.

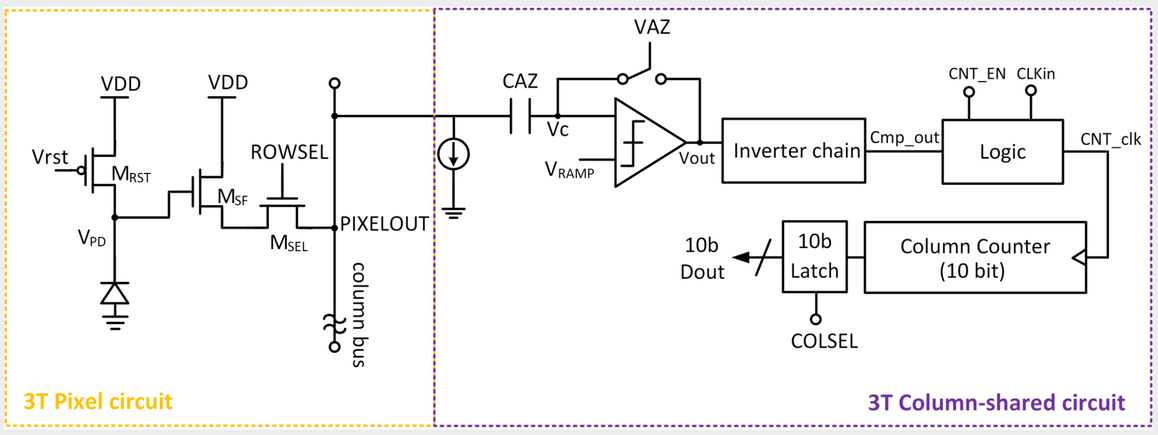


Fig2. 3T-pixel circuit & its readout circuit

The output of a 3T-pixel is the voltage representing photodiode exposure, requiring the column-shared circuit on the 3T-pixel side to utilize a single-slope ADC to convert the voltage signal into a pulse-width signal.

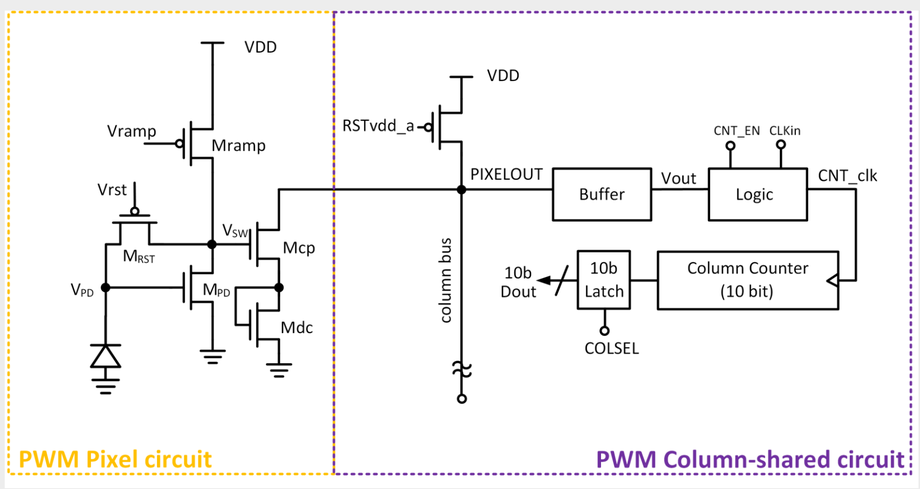


Fig3. PWM-pixel circuit & its readout circuit

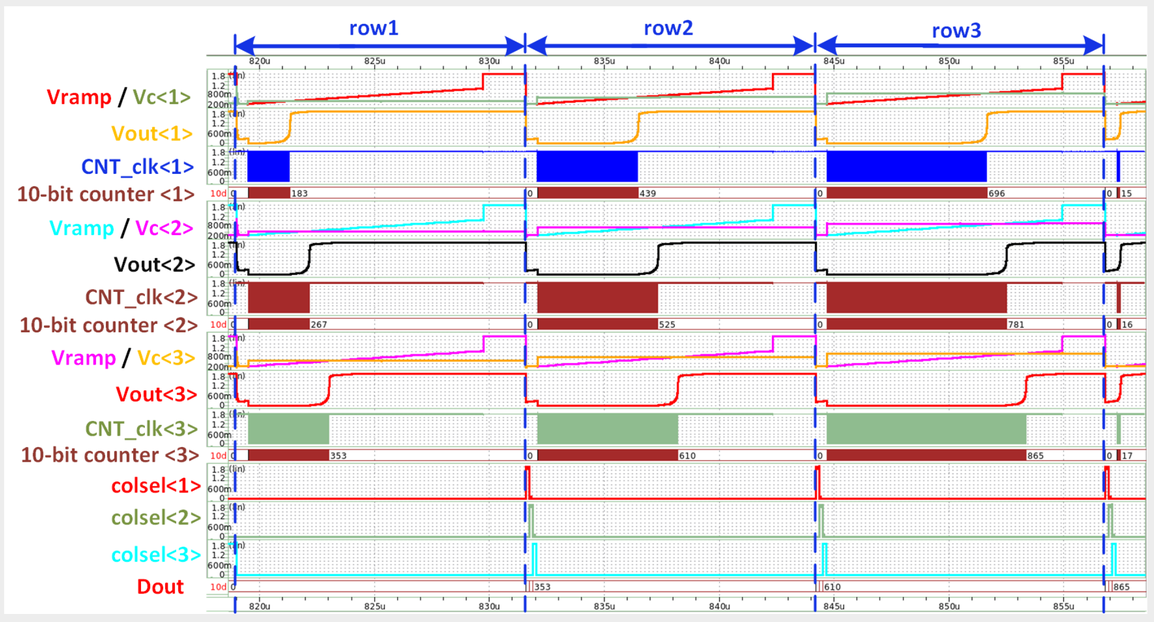
PWM-pixel incorporates an in-pixel comparator, which directly convert the voltage domain photodiode signal into a pulse-width signal as its output.

The pulse-width signals of 3T/PWM pixel are then converted into digital codes using a 10-bit counter. With **rolling shutter** readout method, as the transition moves to the next row, the column control circuit generates a COLSEL signal to output the digital codes from each column.

Result

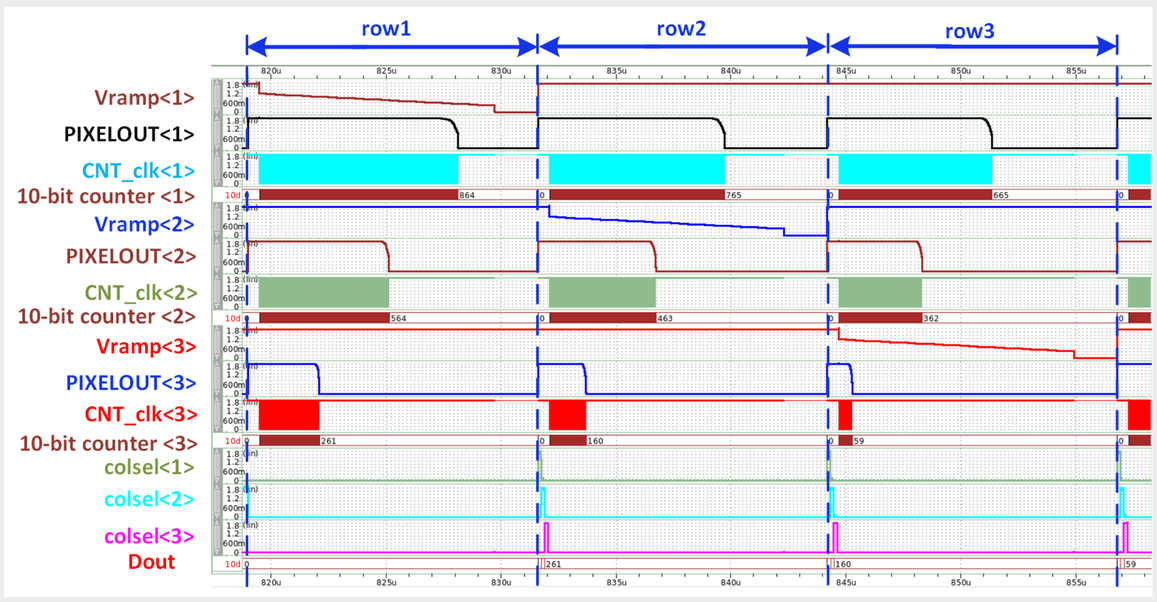
We simplified the 64x64 pixel array into a 3x3 pixel array for simulation purposes. The photodiode in each pixel was modeled using a 50 fF capacitor with a specified photocurrent (Ipd) to simulate illumination. The simulation utilized the Vramp signal generated by the ramp generator.

We captured the 10-bit digital output codes under different Ipd and process corners, then evaluated the linearity using INL (best-fit) method.



Unit: LSB	TT	FF	SS	SF	FS
INL(postsim)	±0.888	±2.9289	±3.0701	±7.1833	±1.4286

Fig4. 3T-pixel simulation waveform & INL under different conditions



Unit: LSB	TT	FF	SS	SF	FS
INL(postsim)	±3.3596	±6.6373	±0.7417	±2.547	±3.5457

Fig5. PWM-pixel simulation waveform & INL under different conditions

Conclusion

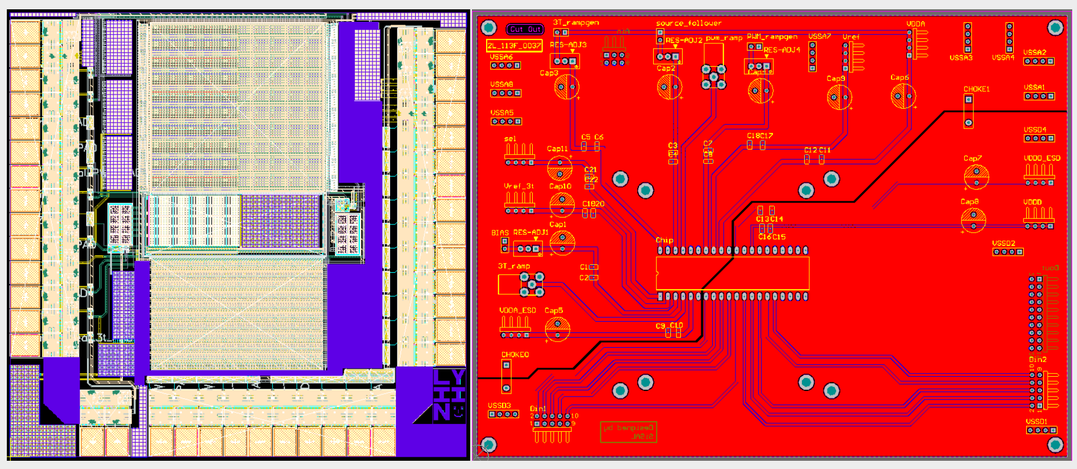


Fig6. Full-chip layout & PCB layout

We successfully integrated two different types of image sensors (3T and PWM) onto a single chip. The design achieves linearity within a similar photocurrent range, with both 3T and PWM reaching INL of ±2 LSB and ±4 LSB, respectively, in TT corner under both pre-simulation and post-simulation.