自舉式開關與單位電容加開關之7-bit循續漸近式類比數位轉換器
7bit SAR ADC with Switch-bootstrapping, USPC DAC

組別：B465　　指導教授：鄭桂忠　　組員姓名：王庭佑、張祐佳、蘇芃睿

Introduction

The Successive Approximation Register Analog-to-Digital Converter (SAR ADC), with its simple structure, high resolution, and superior energy efficiency, has become the preferred solution in various applications in modern electronic devices. This project employs the T18 process, referencing the circuit architecture from the reference [1]. The design achieves the maximum sampling frequency for this structure under the T18 process, while maintaining a compact size and simple logic.

Operating principle

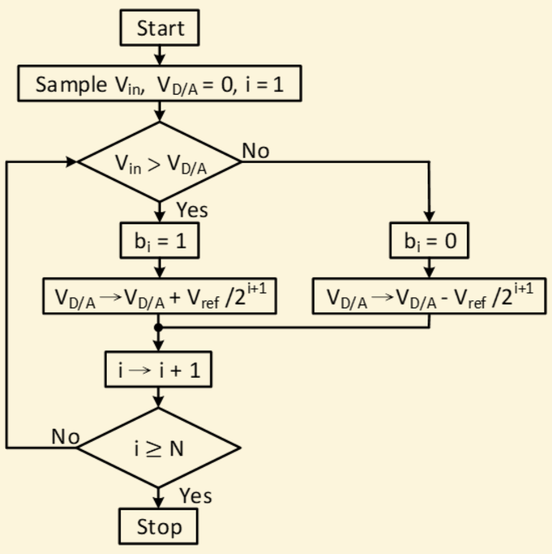

Fig. 1. SAR ADC conversion flow
(From reference [7])

The SAR ADC uses circuitry to implement a binary search algorithm to convert analog signals into digital signal representations.

In each step, the SAR ADC determines if the DAC (digital to analog converter) value is higher or lower than the input voltage. If the DAC's output is less than the input, the bit is set to '1'; if it's greater, the bit is set to '0'.

Circuit architecture

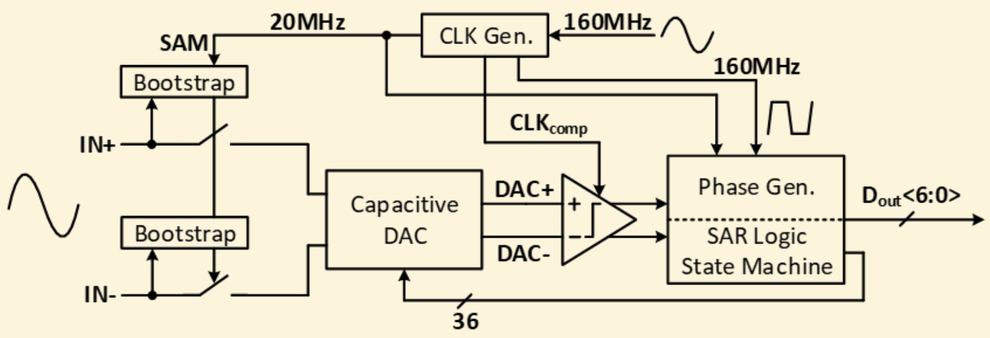

Fig. 2. block diagram

The SAR ADC consists of a sample and hold circuit, a comparator, an SAR logic state machine, a clock generator, and a pair of USPC-DAC (Unit Switch Plus Capacitor Digital-to-Analog Converter).

Results

With the matlab analysis, Post-layout simulation still reaches ENOB(Effective number of bits:$\frac{(SNR-1.76)}{6.02}$) greater than 6.5 bits, which meets the spec.

	corner	ENOB	
specification	all	>6.5	>6.5
Results (pre/post sim)	TT	6.946	6.912
	FF	6.923	7.072
	SS	6.955	6.957
	FS	6.944	7.045
	SF	6.947	6.919

Table. 1. ENOB

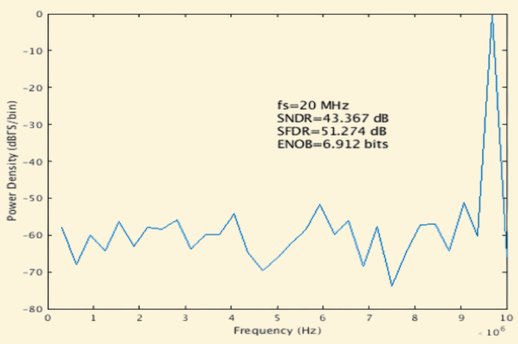

Fig. 6. The FFT spectrum

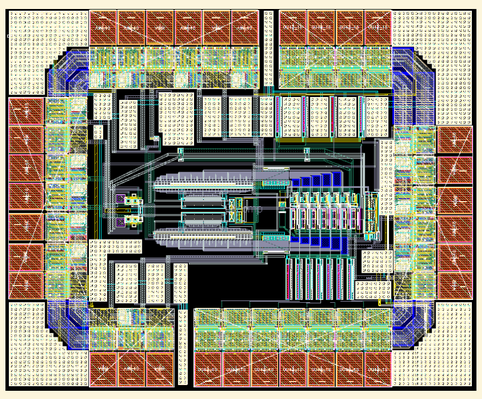

Fig. 7. The layout

Sub-block features

- Semi-Asynchronous Timing
  Fixed cycles
  → Simple logic and smaller area.
  Delay Overlapping for different phases
  → Saving time to increase sampling rate.

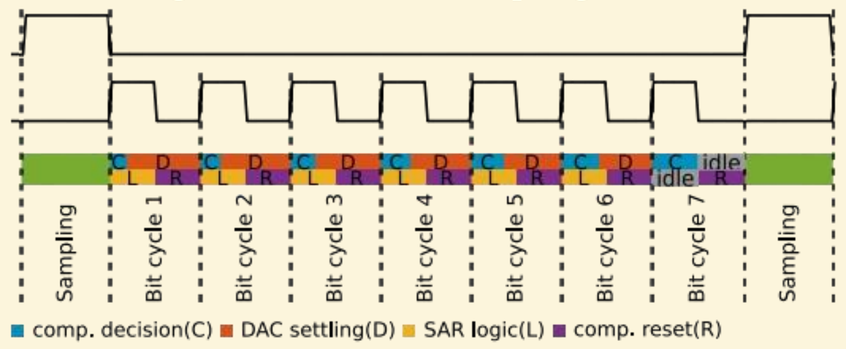

Fig. 3. Semi-Asynchronous Timing With Delay Overlapping
(From reference [1])

- USPC(Unit Switch Plus Capacitor) DAC
  Resistance and capacitance on wirings minimized
  →Faster and more uniformly settling.
  Vcm-based top plate sampling method used
  → Smaller area and easier design for comparator.

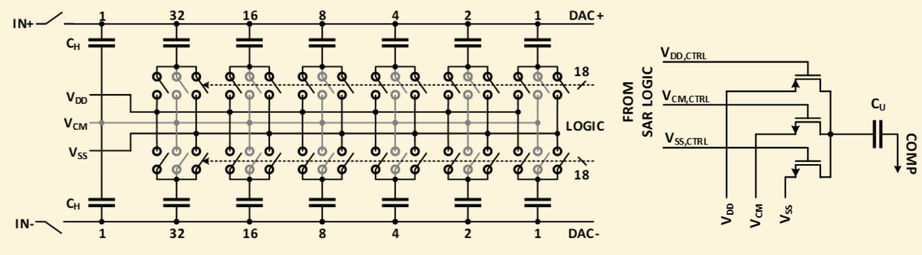

Fig. 4. capacitive DAC and USPC cell schematic

- Triple-Tail Dynamic Comparator
  Dynamic architecture
  → No static power consumption.
  One more stage between preamplifier and latch
  → Shorter comparison time and higher accuracy.

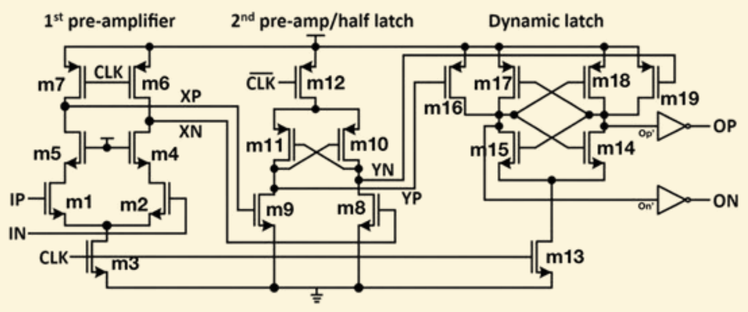

Fig. 5. Triple-Tail Dynamic Comparator schematic

Conclusion

This project successfully implemented a 7-bit SAR ADC based on the T18 process. Simulation results show that the SAR ADC maintains ENOB greater than 6.5 and demonstrates stable performance at a sampling frequency of 20 MHz.

However, the operating speed of the SAR ADC is limited by the DAC capacitors. Increasing the size of the DAC switch transistors improves the operating speed, but parasitic capacitance restricts the effectiveness. Therefore, future research could focus on implementing asynchronous architecture to make good use of conversion times per bit. It can also be extended to time-interleaved architecture in the future.

Reference

[1] Ramkaj, A. T., Strackx, M., Steyaert, M. S. j., & Tavernier, F. (2018). A 1.25-GS/s 7-b SAR ADC With 36.4-DB SNDR at 5 GHz Using Switch-Bootstrapping, USPC DAC and Triple-Tail Comparator in 28-Nm CMOS. *IEEE Journal of Solid-State Circuits*, *53*(7), 74.

[2] Abozeid, K. M., Khalil, A. H., & Aboudina, mohamed M. (2014). Different Configurations for Dynamic Latched Comparators Used in Ultra Low Power Analog to Digital Converters. *2014 International Conference on Engineering and Technology (ICET)*.

[3] dortz, N. L., Blanc, J. P., Simon, T., Verhaeren, S., Rouat, E., Urard, pascal , Tual, S. L., Goguet, D., Perrault, C. lelandais, & Benabes, P. (2014). 22.5 A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs below 70dBFS. *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*.

[4] Razavi, behzad . (2015). The Bootstrapped Switch [A Circuit for All Seasons]. IEEE Solid-State Circuits Magazine, 7(3), 12–15.

[5] Lee, S., Kang, H., & Lee, M. (2024). 9.9 A 2.72fJ/Conv 13b 2MS/s SAR ADC Using Dynamic Capacitive Comparator with Wide Input Common Mode. IEEE International Solid-State Circuits Conference (ISSCC).

[6] Tao, Y., Gu, M., Chi, B., Zhong, Y., & Jie, L. (2024). 22.4 A 4.8GS/s 7-ENoB Time-Interleaved SAR ADC with Dither-Based Background Timing-Skew Calibration and Bit-Distribution-Based Background Ping-Pong Comparator Offset Calibration. IEEE International Solid-State Circuits Conference (ISSCC).

[7] carusone, tony Chan, Johns, D., & Martin, K. (2012). *Analog Integrated Circuit Design Second Edition*. John Wiley & Sons.