CMOS 邏輯相容的非揮發性記憶單元測量與分析

Measurement and Analysis of CMOS Logic Compatible Non-Volatile Memory Cell

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Abstract

With understanding the operational characteristics of Neobit as the core objective, the study analyzes the basic properties of NMOS and PMOS, observes the impact of channel length and secondary effects on the devices, and investigates the gate injection current. Additionally, the research includes basic characterization of T18 Neobit devices.

Samples & Operation principle

NMOS basic characteristic

Utilizing T18 NMOS & N28 PMOS to measure the component characteristics of different device geometrics and perform subsequent analysis.

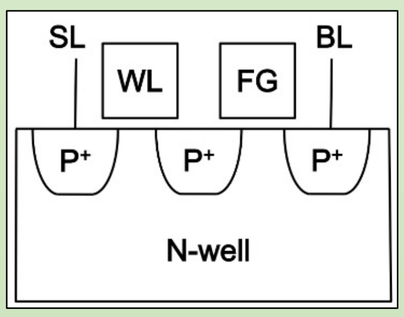
Width	*Length*				
Case1: $W = 10\mu m$	$L = 10\mu m$	$L = 1\mu m$	$L = 0.5\mu m$	$L = 0.22\mu m$	$L = 0.18\mu m$
Case2: $W = 0.5\mu m$	$L = 0.5\mu m$	$L = 0.22\mu m$	$L = 0.18\mu m$		
Case3: $W = 0.22\mu m$	$L = 0.5\mu m$	$L = 0.22\mu m$	$L = 0.18\mu m$		
Length	*Width*				
Case4: $L = 0.22\mu m$	$W = 10\mu m$	$W = 1\mu m$	$W = 0.5\mu m$	$W = 0.22\mu m$	$W = 0.18\mu m$

Electron injection into gate characteristics

Using N16 PMOS with aspect ratio $W/L = 5fin/72nm$ core components to observe gate injection current under different mechanisms.

What is Neobit?

Neobit is a one-time programmable device which is logic compatible. It consists of two PMOS in series and one gate is floating to store data.



↑**Neobit structure**

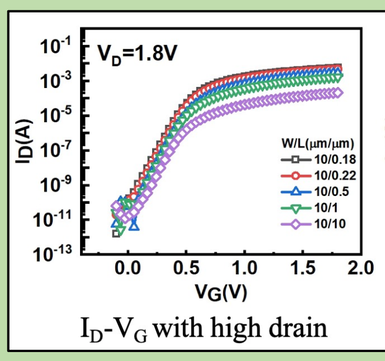
Neobit operating principle

Using T18 process Neobit to study the characteristics before and after program. Injected electrons on FG change the state of a cell.

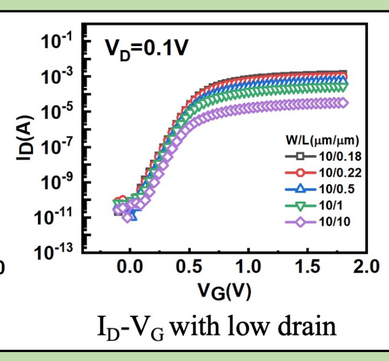
Transistor's Geometric Effect

T18 NMOS measurement

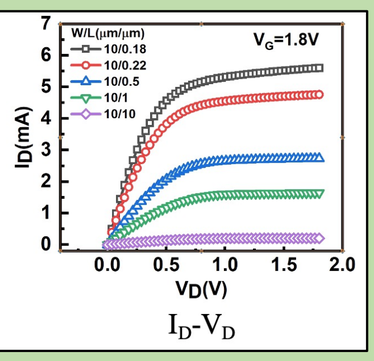
As expected, the devices exhibit characteristics in accordance with the trends of NMOS under different voltages.



I_D-V_G with high drain



I_D-V_G with low drain

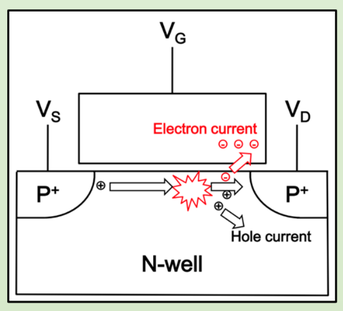


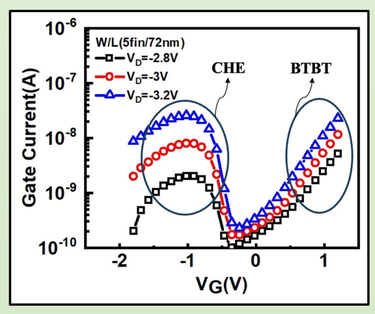
I_D-V_D

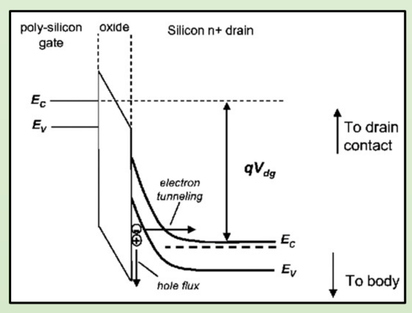
Neobit

Mechanism of electron injection

The two main electron injection mechanisms are CHE (Channel Hot Electron) and BTBT (Band-to-Band Tunneling). CHE occurs when carriers in the channel gain high energy and undergo impact ionization at the drain end of the PN junction, leading to the generation of electron-hole pairs, with electrons injected into the gate. BTBT occurs due to the significant voltage difference formed by high drain and gate voltages, causing a drastic band bending.

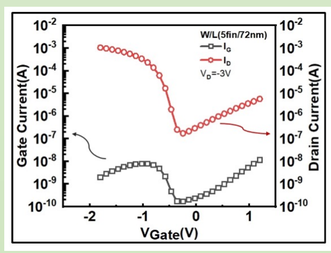


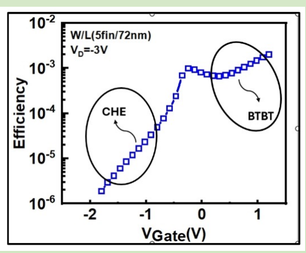




Electron injection efficiency

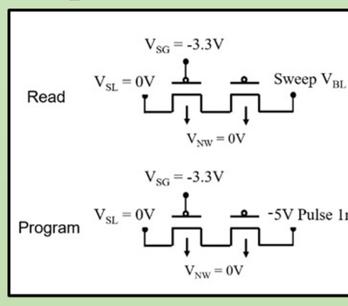
By dividing the gate current by the drain current, one can obtain the electron injection efficiency. The efficiency of CHE is lower than that of BTBT.

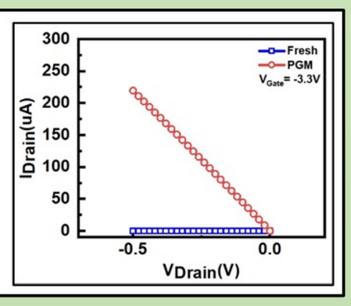


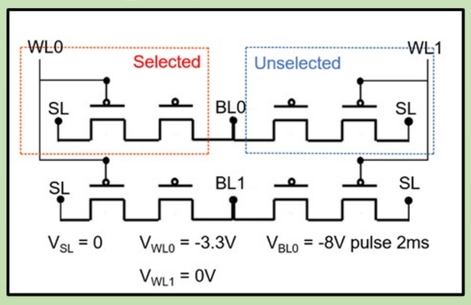


Neobit operation & disturbance

In a Neobit array, if a cell is selected for programming, other cells sharing the same bit line may still be programmed due to the potential difference, which is referred to as program disturb.

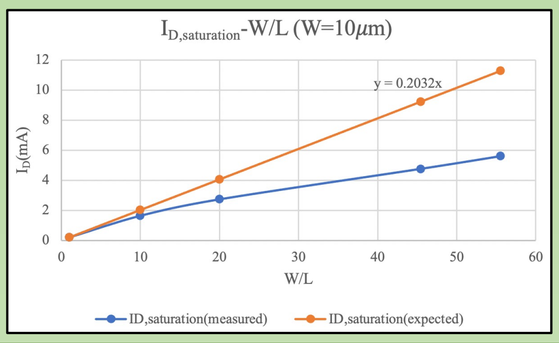


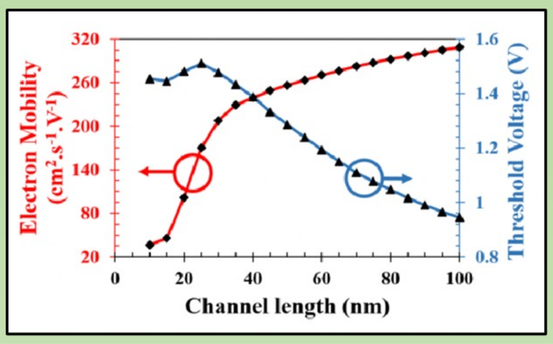




Drain saturation current v.s. aspect ratio

Basic on first-principle model, drain current should be directly proportional W/L, yet there's a slight deviation between the measured value and the ideal value. This deviation can primarily be attributed to the shorter channel length. It causes electron velocity (v=μE) to saturate under high electric fields, resulting in a decrease in electron mobility.





Conclusion

This project studies NMOS with 180nm process and PMOS with 28nm process for basic electrical analysis. In the discussion of drain current versus W/L, electron velocity saturation caused by short channel length leads to non-linear growth.

In the electron injection into gate measurement using PMOS in 16nm process, the significant gate leakage currents occur, attributed to the CHE and BTBT mechanisms, respectively. In comparison, the CHE mechanism offers better cell selectivity, making it more commonly applied as the main program scheme.