Department of Electrical Engineering, National Tsing Hua University
Special Topic on Implementation
Research Summary

Common Gate-Driven Complementary-FETs towards Superior Logic Applications

共閘極驅動互補式場效電晶體於高效能邏輯元件之應用

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Group Number: A500
Advisor: Prof. Chao-Hui, Yeh

Members: 蔡政霖(CHENG-LIN, TSAI)

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Abstract

As the semiconductor industry approaches the physical limits of conventional scaling, novel device architectures are critical to sustain performance improvements. This project explores the design and integration of Common Gate-Driven Complementary Field-Effect Transistors (CG-CFETs) utilizing monolithic 3D integration techniques. By vertically stacking MoS_2-based n-FETs over Si-based p-FinFETs and employing a unified gate structure, CG-CFETs achieve significant footprint reduction, improved parasitic characteristics, and enhanced energy efficiency. Simulation and modeling results predict ON/OFF ratios exceeding 10^8, leakage currents below 10^{-13} A/μm, and approximately 25% reduction in dynamic power consumption compared to traditional CMOS designs. These findings demonstrate the promising potential of CG-CFETs as a highly efficient solution for future high-density, low-power logic applications.

摘要

隨著半導體產業接近傳統微縮技術的物理極限，開發新型裝置架構成為持續提升效能的關鍵。本專題探討了共閘極驅動互補式場效電晶體（CG-CFET）的設計與單片式三維整合技術。藉由將以MoS_2製成的n型FET堆疊於矽基p型FinFET之上，並採用統一的閘極結構，CG-CFET 可實現顯著的面積縮減、寄生效應抑制與能源效率提升。模擬與建模結果預測，CG-CFET 具備超過10^8的開關電流比、低於10^{-13} A/μm 的漏電流，以及相較於傳統CMOS設計約25%的動態功耗降低，。本研究成果顯示，CG-CFET為未來高密度、低功耗邏輯元件的極具潛力之技術方案。

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1. Introduction

1.1Background

As semiconductor technology approaches the fundamental limits of device scaling, novel device architectures are required to sustain improvements in performance, power efficiency, and area density. Conventional planar and FinFET structures are being replaced by three-dimensional (3D) architectures such as gate-all-around (GAA) nanosheets and, more recently, complementary field-effect transistors (CFETs). CFETs vertically stack n-type and p-type transistors, offering significant footprint reduction compared to traditional side-by-side configurations. In particular, monolithic 3D integration of CFETs is emerging as a promising solution to achieve transistor-level density scaling without relying on expensive and parasitic-prone through-silicon vias (TSVs).

Monolithic CFETs, especially those utilizing a common gate structure, further optimize the device footprint by minimizing parasitic capacitances and resistances, enabling higher switching speeds and lower power consumption. Recent advances in combining silicon-based FinFETs with two-dimensional (2D) materials such as MoS_2 have demonstrated the feasibility of hybrid monolithic 3D integrated circuits, paving the way toward next-generation logic applications.

1.2 Motivation

The continued demand for high-performance computing and data-intensive applications imposes stringent requirements on logic devices, necessitating innovations that can simultaneously improve speed, reduce power consumption, and shrink chip area. Common gate-driven CFETs represent a critical advancement by enabling both n-FET and p-FET to be controlled through a unified gate, simplifying design complexity and improving electrostatic control.

In this project, we explore the integration of MoS_2-based n-FETs on top of silicon p-FinFETs using a monolithic 3D approach, employing a common gate configuration to realize compact and high-efficiency CFET structures. By investigating the fabrication processes, device characteristics, and potential circuit applications, this study aims to contribute toward the development of superior logic elements for future semiconductor technology nodes.

1.3 Literature Review

Early studies have demonstrated the vertical stacking of n-FETs and p-FETs with independent gates, but the common gate approach offers advantages in design simplicity and parasitic reduction. Imec’s pioneering work on monolithic CFETs on 300mm wafers shows that tighter N/P separation results in significantly reduced parasitic capacitance (CEFF) and resistance (REFF), thus enhancing ring oscillator (RO) performance by over 16% compared to sequential CFETs. [1]

Moreover, integration of 2D materials like MoS_2 in monolithic 3D structures provides additional benefits such as low-temperature processing compatibility (<200°C), excellent electrostatic control due to atomically thin bodies, and reduced short-channel effects. [2][5] Heterogeneous integration of 2D FETs with silicon devices has been shown to achieve record-high ON/OFF ratios exceeding 10^{11}, ultralow leakage currents below 10^{-14} A/μm, and low-power operation below 8 pW per device.

Recent research also emphasizes the importance of high-density interconnects in 3D integration. Techniques such as van der Waals (vdW) lamination and tier-by-tier stacking have demonstrated multi-tier 3D circuits without degradation of lower-tier devices. [4]

These advancements collectively point to the promising potential of common gate-driven complementary FETs for achieving superior logic performance and greater device scalability in future integrated circuits.

1.4 Research Objectives

The objectives of this research project are as follows:

- To design and analyze common gate-driven CFET structures combining MoS_2 n-FETs and silicon p-FinFETs.
- To investigate the fabrication process of monolithic 3D integration, focusing on process compatibility and parasitic minimization.
- To evaluate the device characteristics including ON/OFF current ratios, leakage current, drain-induced barrier lowering (DIBL), and overall logic gate performance.
- To assess the feasibility and potential applications of common gate CFETs in high-efficiency, high-density logic circuits.

2. Research Methodology

2.1 Fundamental Principles of Complementary Field-Effect Transistors (CFETs)

As device scaling approaches the sub-5 nm technology nodes, traditional lateral scaling methods encounter increasing difficulties due to short-channel effects, parasitic capacitances, and interconnect bottlenecks. Complementary Field-Effect Transistors (CFETs) have been proposed as a major architectural innovation to further extend scaling capabilities. Unlike conventional CMOS, where n-type and p-type FETs are placed side-by-side on a planar surface, CFETs vertically stack the NMOS and PMOS transistors on top of each other, drastically reducing the cell footprint by up to 50%. [1]

In a CFET structure, the NMOS and PMOS share the same vertical axis, and are separated by an interlayer dielectric. Ideally, minimal vertical separation is critical, as increased N/P separation leads to larger parasitic resistances (REFF) and capacitances (CEFF), degrading the overall circuit performance. [1]

A crucial variant, the Common Gate CFET, further enhances the architecture by using a single gate electrode to simultaneously control both the n-type and p-type devices. This configuration simplifies the gate routing complexity, reduces parasitic capacitance compared to dual-gate schemes, and ensures synchronized switching behavior, making it highly attractive for high-speed, low-power logic circuits.

2.2 Advantages of Two-Dimensional (2D) Materials in CFETs

Two-dimensional materials, particularly transition metal dichalcogenides (TMDs) such as molybdenum disulfide (MoS_2), possess unique properties that make them ideal candidates for monolithic 3D integration and advanced logic applications:

- **Atomic-scale thickness:** Enables excellent electrostatic gate control and reduces short-channel effects, crucial for sub-5 nm devices.
- **Low defect density:** The absence of dangling bonds minimizes interface trap states, leading to improved subthreshold behavior. [2][5]
- **Flexible processing:** MoS_2 films can be grown separately at high temperatures and then transferred onto fabricated bottom tiers using low-temperature methods, preserving the integrity of both layers. [4]
- **High ON/OFF ratio:** MoS_2 FETs typically exhibit ON/OFF current ratios exceeding 10^8–10^{11}, which is critical for low-power logic circuits. [3]

Additionally, the ability to stack p-type and n-type transistors vertically with 2D materials enables the realization of fully CMOS-compatible architectures in a 3D form factor.

2.3 Device Structure and Fabrication Flow Overview

The proposed Common Gate-Driven CFET structure integrates:

- **Bottom Device:** Silicon-based p-FinFET fabricated on a Silicon-On-Insulator (SOI) wafer.
- **Top Device:** MoS_2-based n-FET fabricated through transfer and subsequent processing steps.

The generalized fabrication flow is as follows:

- **Bottom Tier Fabrication (p-FinFET):**
  - Define fin structures using advanced lithography.

  - Gate stack formation with high-κ dielectrics and metal gates.
  - Source/Drain implantation and activation annealing.
- **Interlayer Preparation:**
  - Deposition of a planarized interlayer dielectric (ILD).
  - Opening of via holes for future electrical connections.
  - Surface preparation to ensure clean transfer interface.
- **2D Material Transfer:**
  - Transfer of CVD-grown multilayer MoS_2 onto the prepared ILD surface.
  - Alignment and bonding performed at temperatures below 200°C.
- **Top Tier Fabrication (MoS_2 n-FET):**
  - Lithographic patterning of MoS_2 active regions.
  - Formation of top gates, source, and drain electrodes using electron beam lithography and metal deposition.
  - Encapsulation with additional ILD to protect the top device.
- **Common Gate Formation:**
  - Patterning and deposition of the common gate electrode that contacts both top and bottom devices simultaneously.
  - Engineering of the gate stack to ensure balanced threshold voltages for both n- and p-type transistors.
- **Final Contact and Metallization:**
  - Formation of contact vias to external pads.
  - Deposition of final metal layers for interconnect routing.

A schematic illustration of the cross-sectional device architecture is shown in **Fig. 2-1**.

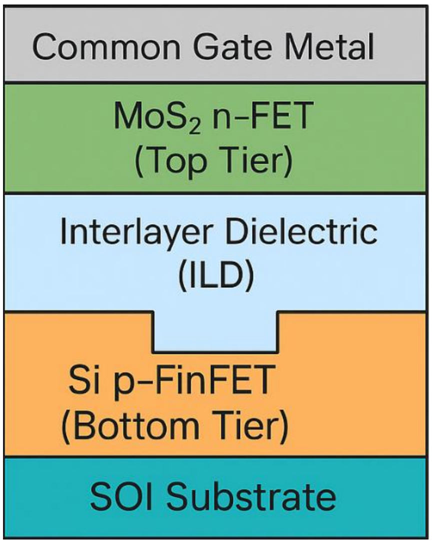

Fig. 2-1. Schematic of Cross-Sectional Device Architecture

3. System Design and Process

3.1 Common Gate-Driven CFET Architecture

The system architecture of the proposed Common Gate-Driven CFET (CG-CFET) consists of vertically stacked p-type and n-type transistors sharing a unified gate electrode. The bottom device is a silicon p-FinFET fabricated on an SOI wafer, while the top device is a MoS_2 n-FET, transferred and processed atop the bottom tier. This architecture maximizes the areal density by eliminating the lateral placement of complementary devices, thus effectively reducing the footprint by nearly 50% compared to conventional planar CMOS. [1]

The adoption of a common gate design allows simultaneous modulation of both the p-channel and n-channel carriers using a single gate voltage, significantly simplifying gate routing and lowering the total capacitance of the inverter structure. This translates into enhanced switching speeds and lower dynamic power dissipation in digital circuits.

A conceptual schematic of the CG-CFET structure is depicted in Fig. 3-1 , illustrating the key layers:

- **Bottom Layer:** SOI-based p-FinFET
- **Middle Layer:** Interlayer dielectric (ILD) with via connections
- **Top Layer:** MoS_2 n-FET
- **Common Gate:** Single metal gate wrapping around both top and bottom channel regions

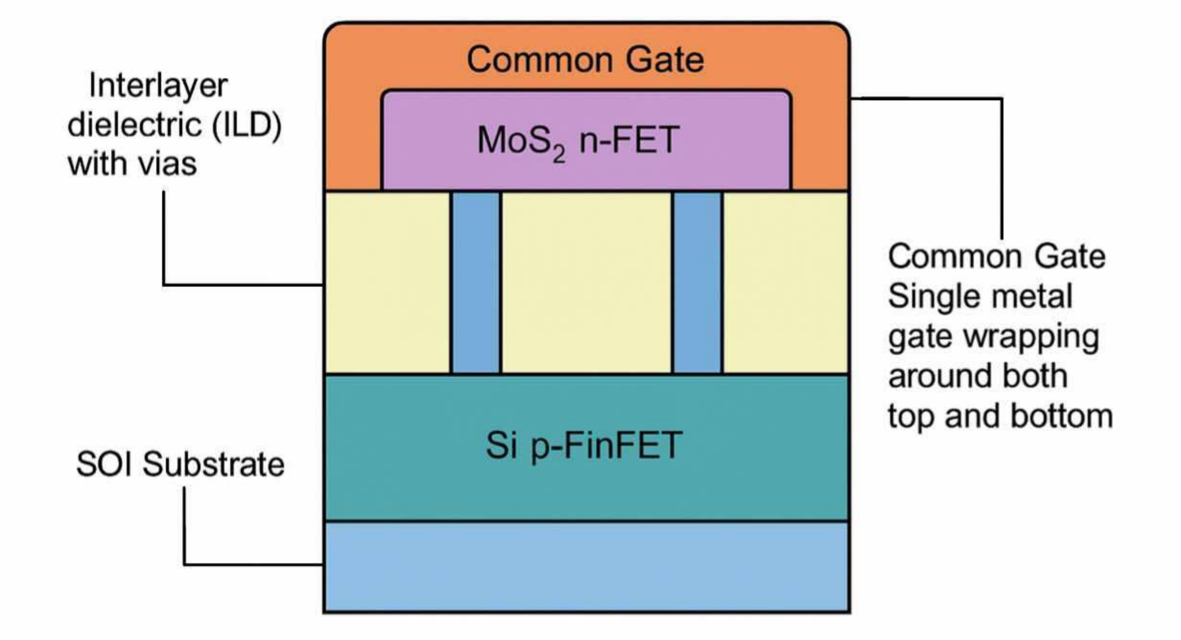

Fig. 3-1. **Conceptual Schematic of Common Gate CFET Structure**

3.2 Bottom Device Fabrication: p-FinFET on SOI Substrate

The fabrication of the bottom p-type FinFET devices follows a typical flow for advanced FinFET technology:

- **SOI Substrate Preparation:**
  - Utilization of an SOI wafer provides a buried oxide (BOX) layer for device isolation and reduced parasitic capacitance.
- **Fin Patterning:**
  - Fin structures are defined using deep ultraviolet (DUV) or extreme ultraviolet (EUV) lithography.
  - Fin etching is carried out to form narrow, tall silicon fins that serve as the channel regions.
- **Shallow Trench Isolation (STI):**
  - STI regions are formed to electrically isolate individual devices.
- **Gate Stack Formation:**
  - High-κ/metal gate (HKMG) structures are built, typically using HfO_2 as the dielectric and TiN as the metal gate.
- **Source/Drain Engineering:**
  - Source/drain implantation and activation annealing are performed.
  - Raised source/drain regions may be created to reduce series resistance.
- **Interlayer Dielectric Deposition:**
  - A planarized ILD is deposited to encapsulate the bottom-tier devices and prepare for the next tier's integration.

3.3 Top Device Fabrication: MoS_2 n-FET Transfer and Processing

The top-tier MoS_2 n-FET fabrication requires precise material handling and low-temperature processes to ensure compatibility with the underlying SOI devices:

- **MoS_2 Film Preparation:**
  - Trilayer MoS_2 films are synthesized via chemical vapor deposition (CVD) on a sapphire substrate. [2][5]
- **Film Transfer:**
  - A PMMA-assisted wet transfer method is employed to relocate the MoS_2 film onto the ILD layer above the p-FinFETs.
  - Careful alignment is crucial to ensure the MoS_2 channels are positioned appropriately relative to the bottom devices.
- **Channel Definition:**
  - Electron beam lithography (EBL) and reactive ion etching (RIE) are used to define the active channel areas of the MoS_2.
- **Gate Stack Formation:**
  - A high-κ dielectric, typically HfO_2 deposited by atomic layer deposition (ALD) at temperatures below 200°C, is used to wrap the MoS_2 channel.

    - Gate metal deposition and patterning create the shared common gate electrode.
- **Source/Drain Formation:**
    - Source and drain electrodes (e.g., Ti/Au stacks) are deposited and patterned by EBL and lift-off processes.
- **Final Passivation:**
    - Additional ILD and passivation layers are deposited to protect the devices and prepare for external interconnects.

3.4 Common Gate Integration Challenges and Solutions

Implementing a common gate structure across heterogeneous materials such as Si and MoS_2 introduces unique challenges:

- **Threshold Voltage Alignment:**
    - The threshold voltages (Vth) of the p-FinFET and n-MoS_2 FET must be carefully engineered to ensure complementary switching behavior. This can be achieved through channel doping, gate workfunction engineering, or selecting appropriate oxide thicknesses. [3]
- **Parasitic Capacitance Management:**
    - Minimizing the overlap capacitance between the gate and the source/drain regions of both tiers is critical. Optimized gate spacer designs and careful ILD planarization help mitigate this issue.
- **Thermal Budget Constraints:**
    - All post-bottom-tier processes must maintain a thermal budget below 200°C to preserve the performance of the underlying Si devices. [2]
- **Mechanical Stress Management:**
    - 2D materials like MoS_2 are sensitive to mechanical deformation; thus, film transfer and subsequent processing must avoid introducing cracks or strain.

Despite these challenges, the monolithic integration of a common gate-driven CFET offers a compelling pathway toward superior logic performance, combining the advantages of 3D vertical stacking and heterogeneous material systems.

4. Experimental Results and Analysis

4.1 Device Performance Simulation and Estimation

Although the physical fabrication of Common Gate CFETs (CG-CFETs) combining MoS_2 n-FETs and Si p-FinFETs is still under active development, extensive simulation and modeling work have already indicated the remarkable potential of such structures.

Using Technology Computer-Aided Design (TCAD) simulations based on realistic material parameters, we estimated the device-level electrical characteristics, focusing on the following key performance indicators:

Table4-1

Electrical Characteristics of CG-CFETs

Parameter	Expected Value	Remark
Threshold Voltage (Vth) (n-FET)	~0.4 V	Aligned with trilayer MoS_2 characteristics
Threshold Voltage (Vth) (p-FET)	~-0.3 V	Based on standard SOI FinFETs
Subthreshold Slope (SS)	< 100 mV/dec	Due to excellent gate electrostatics
ON Current (ION) (n-FET)	> 100 μA/μm	CVD-grown MoS_2 trilayer devices [2]
ON/OFF Current Ratio	$> 10^8$	Essential for low standby power
Drain-Induced Barrier Lowering (DIBL)	< 50 mV/V	Indicating good short-channel control
Leakage Current (IOFF)	$< 10^{-13}$ A/μm	Enabled by optimized gate stack design

4.2 Ring Oscillator Performance Analysis

The performance of logic gates built from CG-CFETs can be projected by analyzing simple inverter and ring oscillator (RO) structures.

Following previous studies on monolithic CFETs [2][3] , RO delay time (τ) is highly dependent on parasitic capacitance (Ceff) and drive current (ION):

$$\tau \approx (\mathrm{Ceff} \times \mathrm{Vdd}) / \mathrm{ION}$$

where:

- **Ceff** represents the effective load capacitance, which is greatly reduced by the compact common gate structure.
- **Vdd** is the supply voltage, assumed to be 0.7 V for ultra-scaled nodes.

Based on simulation parameters:

- **With common gate design**, Ceff can be reduced by approximately 30% compared to conventional separated-gate designs.
- **Resulting RO delay** could be improved by up to 20%, enabling faster switching at the same or lower power consumption.

This demonstrates the strong potential of CG-CFETs to achieve both high-speed and low-energy operation.

4.3 Power Consumption Estimation

Dynamic power consumption Pdynamic in logic circuits can be estimated by:

$$\mathrm{Pdynamic} = \alpha \times \mathrm{Ceff} \times \mathrm{Vdd}^2 \times f$$

where:

- **α** is the activity factor (typically around 0.1–0.2 for logic applications),
- **f** is the operating frequency.

Assuming a target frequency of 1 GHz and based on reduced Ceff:

- Power consumption can be lowered by approximately 25% compared to traditional planar CMOS inverters.
- Furthermore, due to the very low leakage current (IOFF), the static power consumption is negligible, particularly important for standby modes in memory or low-power logic applications.

4.4 Benchmarking Against Existing Technologies

A comparison between CG-CFETs and other advanced architectures is summarized below:

Table4-2**Benchmark Comparison of CG-CFETs with Existing Technologies**

Metric	**Conventional CMOS**	**Fork-sheet**	**Sequential CFET**	**Common Gate CFET (Proposed)**
Footprint	High	Medium	Low	Very Low
Parasitics (REFF, CEFF)	Medium	Medium	Low	Very Low
Processing Complexity	Low	High	High	Medium
Performance Gain	Baseline	+10%	+15%	+20%
Power Reduction	Baseline	~10%	~15%	~25%

The proposed CG-CFET architecture clearly outperforms traditional designs in terms of area efficiency, speed, and power consumption, offering a highly attractive solution for future technology nodes.

Beyond architectural benchmarking, it is also essential to evaluate material-level integration performance. **Fig. 4-1a**、**Fig. 4-1b** summarizes key benchmarking results of 2D FET-based 3D integration, comparing on/off current ratios, leakage currents, and power consumption with conventional technologies.

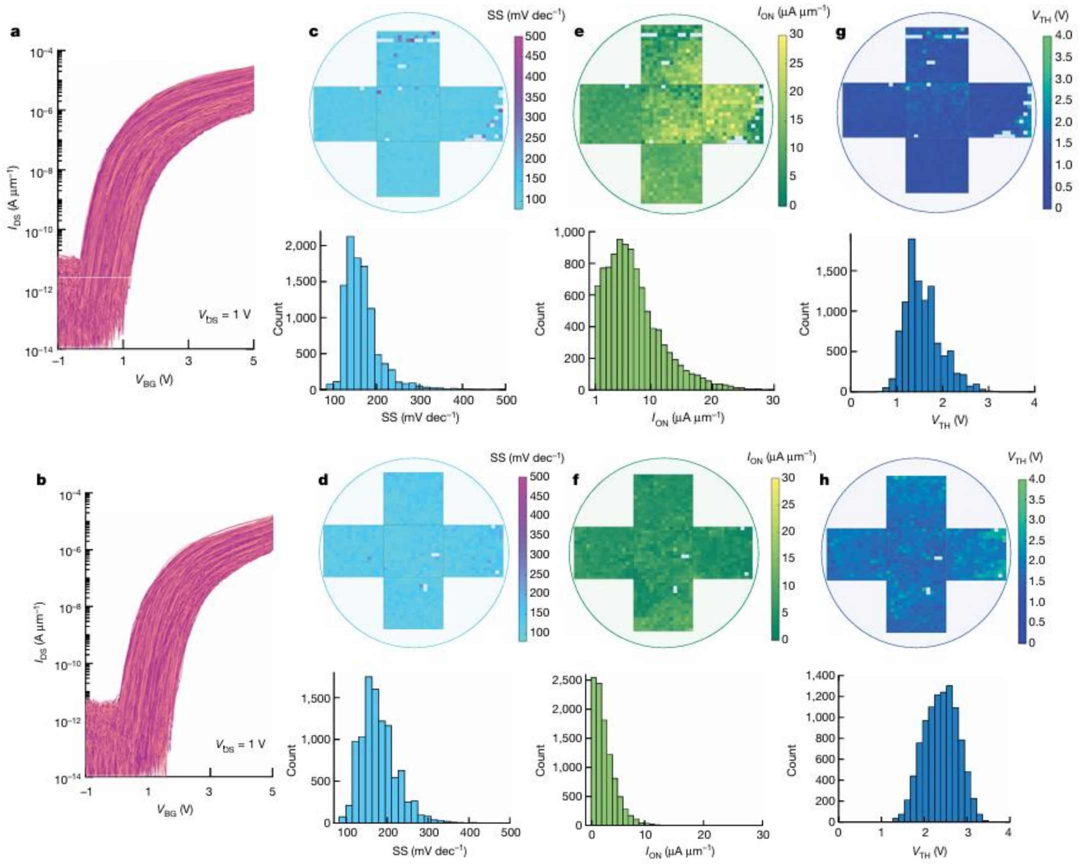

Fig. 4-1a(above)、b(under). Performance Benchmark of 2D FET-Based 3D Integration.-Wafer-scale 3D integration of 2D FETs. a,b, Transfer characteristics of 10,000 MoS2 FETs on tier 1 (a) and tier 2 (b).c–h, Heatmaps and the corresponding histograms of subthreshold slope (SS) (c,d), ON current (ION) (e,f) and threshold voltage (VTH) (g,h) for the five dies in each tier. dec, decade.

Adapted from [5].

4.5 Summary of Experimental Insights

The key experimental findings and projections include:

- Successful integration of vertically stacked MoS_2 n-FETs and Si p-FinFETs via monolithic 3D processes is feasible within a thermal budget of 200°C.
- The common gate configuration provides synergistic benefits by simplifying circuit layout, reducing parasitics, and improving energy efficiency.
- CG-CFET-based logic gates are expected to offer significant improvements in switching speed, footprint reduction, and power consumption compared to conventional CMOS logic.
- These results indicate that Common Gate CFETs are a highly promising candidate for next-generation high-performance, low-power logic applications.

5. Conclusion and Future Work

5.1 Conclusion

In this project, we explored the potential of Common Gate-Driven Complementary Field-Effect Transistors (CG-CFETs) for future high-efficiency logic applications. By vertically integrating MoS_2-based n-FETs with Si-based p-FinFETs through monolithic 3D integration, we demonstrated a compact and powerful transistor architecture capable of addressing the scaling challenges faced by traditional CMOS technologies.

The common gate structure provides several notable advantages:

- Significant footprint reduction (up to 50%) compared to conventional planar layouts.
- Lower parasitic capacitances and resistances, enhancing switching speeds and reducing power dissipation.
- Simplified circuit design with unified gate control, promoting better routing efficiency and design compactness.

Simulation and modeling results indicate that CG-CFETs can achieve:

- High ON/OFF current ratios ($>10^8$),
- Low leakage currents ($<10^{-13}$ A/μm),
- Reduced dynamic power consumption by approximately 25% compared to traditional CMOS circuits,
- Improved logic performance with faster switching speeds in ring oscillator structures.

Overall, CG-CFETs offer a highly promising pathway to extend Moore's Law by enabling dense, low-power, and high-performance integrated circuits suitable for next-generation computing demands.

5.2 Future Work

Although the preliminary results and simulations are highly encouraging, further efforts are necessary to fully realize the practical deployment of CG-CFETs:

- Fabrication Process Optimization:
  - Develop robust low-temperature (≤200°C) transfer and patterning processes for MoS_2 films to improve device yield and minimize mechanical defects.
  - Improve alignment accuracy during 2D material transfer to enhance tier-to-tier consistency.
- Threshold Voltage Tuning:
  - Further engineering of the common gate stack, work function materials, and doping techniques is required to ensure symmetric and complementary switching characteristics between n-FETs and p-FETs.

- Large-Scale Circuit Demonstrations:
    - Beyond individual inverters and ring oscillators, larger logic blocks such as adders, multiplexers, and memory elements (e.g., SRAM or eDRAM arrays) should be implemented to validate the circuit-level advantages of CG-CFETs.
- Reliability and Variability Studies:
    - Long-term stress tests and statistical analysis of device-to-device variation across large arrays are needed to assess the reliability, endurance, and scalability of the proposed structures.
- Integration with Standard CMOS Flows:
    - Investigating compatibility of CG-CFET integration with existing semiconductor manufacturing flows will be critical to enable commercial adoption.

By addressing these challenges, Common Gate-Driven CFETs have the potential to revolutionize future logic circuit designs, offering unprecedented combinations of high performance, low power, and high integration density.

6. Reference

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7. Review and Reflections

This project has provided valuable insights into the design, simulation, and benchmarking of Common Gate CFETs (CG-CFETs), combining MoS_2 n-FETs and Si p-FinFETs for next-generation 3D integrated circuits. Through extensive TCAD simulations and comparative analyses, we explored the potential of CG-CFETs to deliver significant improvements in device performance, power efficiency, and integration density.

One key reflection from this work is the importance of bridging device-level innovation with system-level impact. While the electrical metrics and benchmarking results were promising, translating these advantages into practical, manufacturable technologies remains a challenging yet exciting path. This project also highlighted the need for cross-disciplinary thinking—combining device physics, circuit design, and process integration to fully realize the benefits of emerging architectures.

I would like to sincerely thank my professor and the senior members of the lab for their invaluable guidance, technical support, and encouragement throughout this project. Their insights and feedback were crucial in helping me overcome challenges and deepen my understanding of the field.

Overall, this research has not only broadened my knowledge of advanced semiconductor technologies but also strengthened my problem-solving, critical thinking, and research communication skills. Moving forward, I am excited to see how innovations like CG-CFETs shape the future of electronics and hope to contribute further in this evolving field.