Abstract

Network-on-Chip (NoC) is a network-based communications subsystem on an integrated circuit between modules in a System-on-Chip (SoC). The modules on the IC are semiconductor IP cores schematizing CPU, GPU, DSP, memory and various functions of the computer system, and are designed to be modular in the sense of network science with the advantage of high-speed, efficient, and low latency. Previously, NoC is not that needed for the high-tech companies, but with the development of AI chip, NoC technique becomes more important. However, most of the existing methods to implement NoC are deficient due to high latency and significant power consumption. In order to improve the work, the novel wireless network-on-chip (WiNoC) emerges. Its architecture employs modulated RF carriers to establish single-hop high-speed wireless links for distant cores on a chip. The WiNoC architecture necessitates a highly efficient wireless transceiver that can communicate at a data rate of tens of Gb/s. For a short communication distance of 20 mm, on-off keying (OOK) is one of the most energy efficient modulation schemes due to its low complexity.

As a result, OOK receiver is the topic of our project, which consists of a power detector, a level shifter, and a limit amplifier. OOK denotes the simplest form of ASK modulation that represents digital data as the presence or absence of a carrier wave. The presence of a carrier for a specific duration represents a binary one, while its absence for the same duration represents a binary zero.

Introduction

The proposed OOK receiver includes the following three functional blocks:

1. Power Detector (or Envelope Detector):

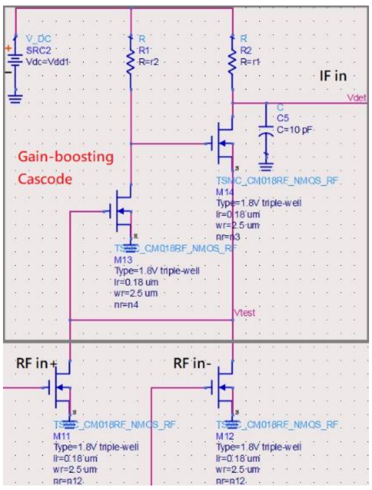

Fig. 1. Power detector

Power detector receives 60 GHz signal and recovers the AM signal from RF carrier. The schematic of the power detector is shown in Fig. 1. To demodulate the signal immediately and precisely, low RC time constant is necessary. However, this could seriously reduce the output impedance, which denotes that the output swing it provides would be obviously suppressed.

Therefore, we utilize "gain-boosting technique". Gain-boosting technique is a common way to offer high gain in RF circuit design. In Fig. 1, a cascode transistor (M_{14}) with an auxiliary gain-boosting amplifier (M_{13} and R_1) is inserted between the load resistor and the drains of M_{11} and M_{12}. By doing so, the conversion gain could be effectively increased by the additional gain of the auxiliary stage.

As the differential signal input, the differential pair gives in-phase envelope signal, while the fundamental signals are cancelled out due to their 180° phase difference. After that, the envelope signal undergoes two-stage amplification, entering the next stage.

2. Level Shifter

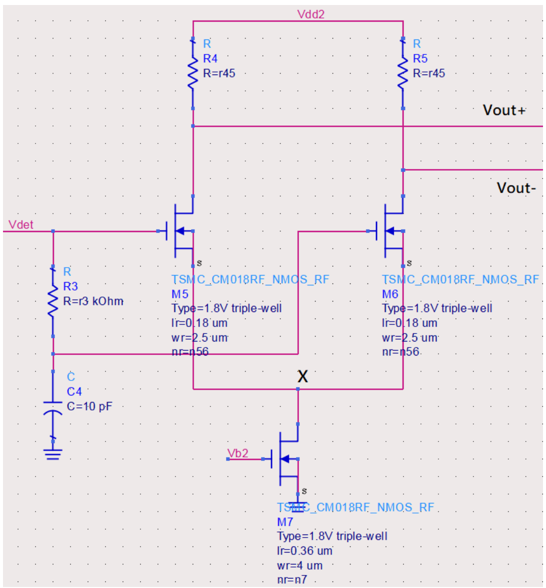

Fig. 2. Level Shifter

Level shifter is a simple structure to shift one dc level to a proper bias. By well-designing the current source and the load resistors, the output dc value can be therefore defined.

The schematic of the level shifter is shown in Fig. 2. In Fig. 2, node X (sources of M_5 and M_6) is AC-grounded in the differential pair. Note that the bias voltage of node X guarantees the operation in saturation of M5/M6/M7. The target output bias voltage, which is required as input voltage of the limiting amplifier, can be simply defined as:

$$V_{out} = VDD - 0.5 I_{M_7} R_{4,5}$$

, where I_{M_7} is the current M_7 flows.

In this design, the level shifter provides a single-ended to differential conversion by simply adding an RC pair at the input. It is important since most following stages, such as baseband amplifier and digital circuits, are designed with differential circuits to eliminate common-mode noise.

3. Limiting Amplifier:

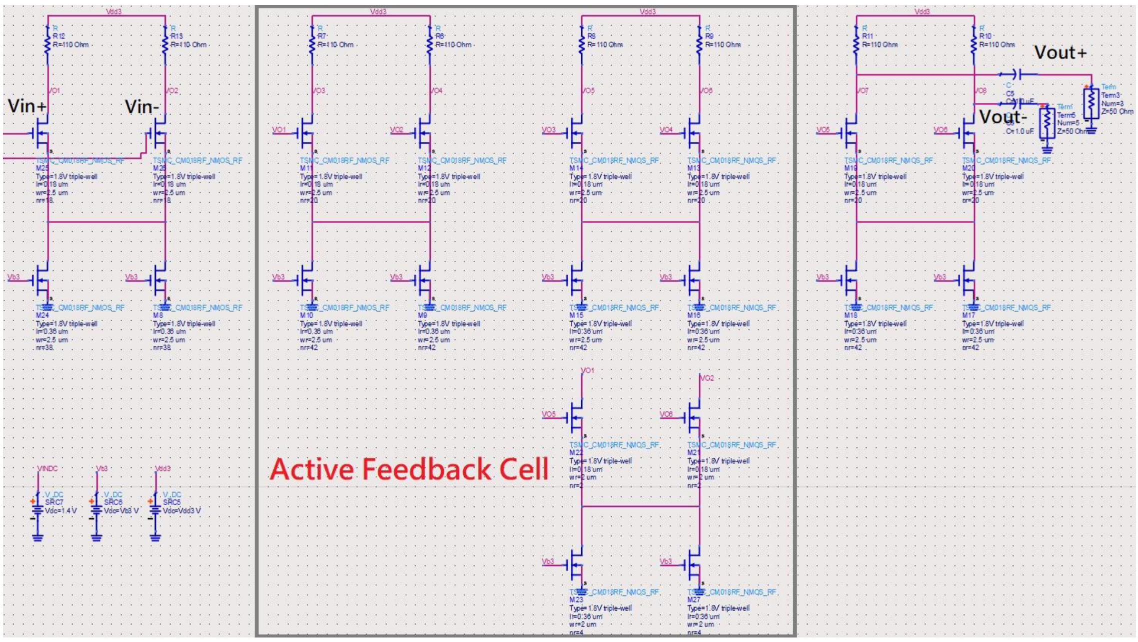

Fig. 3. Limiting Amplifier

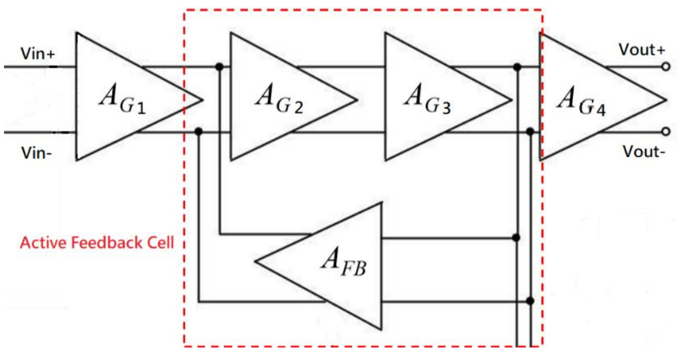

Fig. 4. Block diagram of Limiting Amplifier

Limiting amplifier is used to amplify the envelope signal up to a certain level, which is needed while measuring it with an oscilloscope.

The schematic of the limiting amplifier is shown in Fig. 3, and the block diagram is shown in Fig. 4. In Fig. 4, $A_{G2}/A_{G3}/A_{FB}$ forms a close loop with shunt-shunt feedback connection. Active feedback is a common method to extend the bandwidth with sufficient stability since the dominant pole is pushing to a higher frequency.

Moreover, limiting amplifier provides high gain, which ought to give stable high and low signal, indicating binary ones and zeros, respectively.

心得

在本次的實作專題中，我們學習到如何把課堂上及課本上所學的知識應用在實際設計電路。也了解到套用理論跟公式所計算的結果有時會跟模擬結果、或是預期的結果不太一樣，電路中往往會因為疏忽一個小細節而導致結果大相逕庭，我想這就是需要經驗的累積來增強實力。經過上、下學期的學習及實作後，我們對電路設計有更深一層的了解，而從著手設計的過程中我們知道電路設計的辛苦，但也從中找到一些樂趣，而在成功得到理想的模擬結果後更是會有滿滿的成就感。希望我們能藉著這次經驗，瞭解自己的不足並增進實力，繼續向前邁進。