60-GHz OOK CMOS 接收器之設計

Design of 60-GHz OOK CMOS Receiver

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Abstract

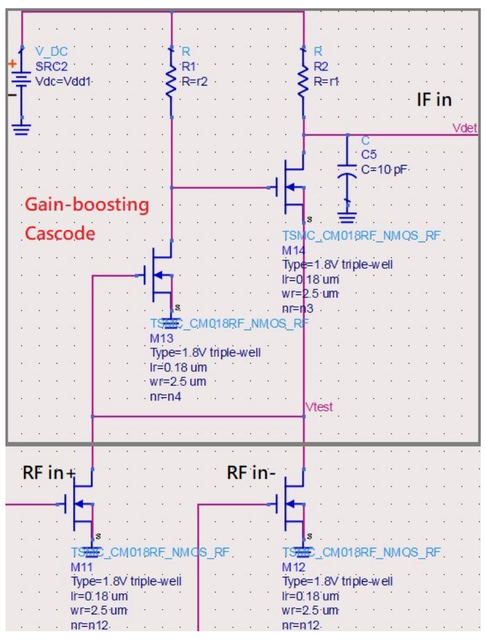
Network-on-Chip (NoC) is a network-based communications subsystem on an integrated circuit between modules in a System-on-Chip (SoC). Previously, NoC is not that needed for the high-tech companies, but with the development of AI chip, NoC technique becomes more important. However, most of the existing methods to implement NoC are deficient due to high latency and significant power consumption. In order to improve the work, the novel wireless network-on-chip (WiNoC) emerges. Its architecture employs modulated RF carriers to establish single-hop high-speed wireless links for distant cores on a chip. The WiNoC architecture necessitates a highly efficient wireless transceiver that can communicate at a data rate of tens of Gb/s. For a short communication distance of 20 mm, on-off keying (OOK) is one of the most energy efficient modulation schemes due to its low complexity.

As a result, OOK receiver is the topic of our project, which consists of a power detector, a level shifter, and a limit amplifier. OOK denotes the simplest form of ASK modulation that represents digital data as the presence or absence of a carrier wave. The presence of a carrier for a specific duration represents a binary one, while its absence for the same duration represents a binary zero.

Implementation

1. Power Detector (or Envelope Detector):

Power detector receives 60 GHz signal and recovers the AM signal from RF carrier. As the differential signal input, the differential pair gives in-phase envelope signal, while the fundamental signals are cancelled out due to their 180 phase difference. After that, the envelope signal undergoes two-stage common-source amplification, entering the next stage.



2. Level Shifter :

Level shifter is a simple structure to shift one dc level to a proper bias. By well-designing the current source and the load resistors, the output dc value can be therefore defined.

The level shifter provides a single-ended to differential conversion by simply adding a RC pair at the input. It is important since most following stages, such as baseband amplifier and digital circuits, are designed with differential circuits to eliminate common-mode noise.

3. Limiting Amplifier :

Limiting amplifier is used to amplify the envelope signal up to a certain level, which is needed while measuring it with an oscilloscope.

In the figure below, there is a close loop with shunt-shunt feedback connection. Active feedback is a common method to extend the bandwidth with sufficient stability since the dominant pole is pushing to a higher frequency.

Moreover, limiting amplifier provides high gain, which ought to give stable high and low signal, indicating binary ones and zeros, respectively.

Result

In our simulation, the input power is set to -20 dBm, which is a common scale at the output of a low-noise amplifier. Also, we set a 5 GHz on-off signal carried by a 60 GHz RF carrier to emulate a 10 Gb/s V-band OOK signal as shown in Fig.1(a). In Fig.1(b), the power detector provides an output swing around 53 mV and namely, a responsivity of 5300 mV/mW at the input power of -20 dBm. This is good enough for the following stage to detect and process. After the envelope signal being detected, it comes to baseband signal processing. The first step is to convert the single-ended signal to differential ones. Thus, a level shifter is applied. As shown in Fig.1(c), the output swing of each node can reach to around 35 mV. Furthermore, it provides a suitable 1.4V-DC level for the following stage. Then here comes to the last stage - the baseband limiting amplifier. This stage is expected to provide high gain, wide bandwidth and high stability. Nonetheless, there are direct trade-offs between them. Therefore, we set the spec of 10 dB AC gain and 5 GHz 3-dB bandwidth, for the10 Gb/s data rate (note that the optimum 3-dB BW is 0.56 data rate = 5.6 GHz). Finally, combine the above components together to form a relatively complete working cell. As the simulated -20 dBm V-band signal with 10 Gb/s is input, the receiver provides a ~200 mV differential output signal. This is quite sufficient for either measurement or providing to the following digital stages. For the total DC power, the RX consumes 78.1 mW. While for each stage, the power detector, level shifter and limiting amplifier consume 2.8 mW, 6.6 mW and 68.7 mW.

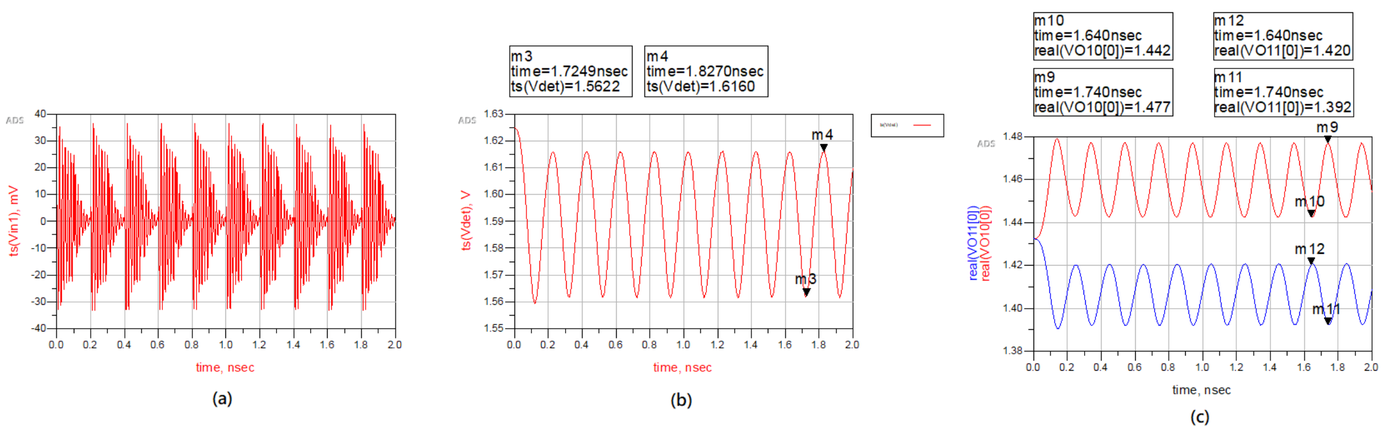


Fig. 1 (a) input signal (b) baseband signal at the output of the power detector (c) baseband

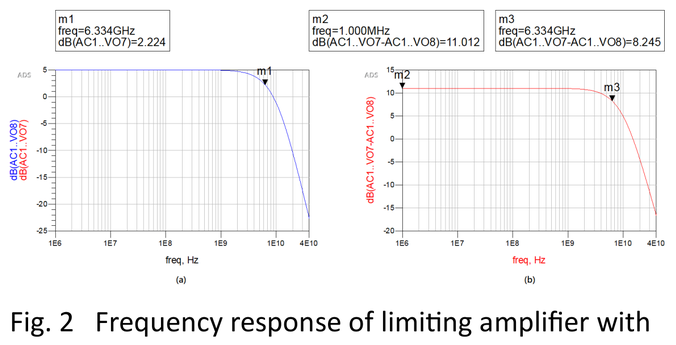


Fig. 2 Frequency response of limiting amplifier with (a) single-ended (b) differential output

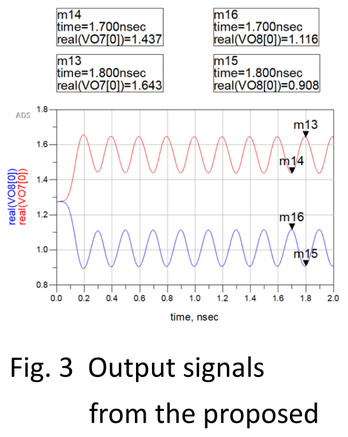


Fig. 3 Output signals from the proposed OOK RX

Conclusion

A 10 Gb/s V-band OOK Rx in 180 nm CMOS process is presented. With the gain-boosting-cascode power detector and baseband amplifier implementation, the RF amplitude modulation signal can be precisely detected and provide to the following stages. As shown in the simulation result, the output node provides ~200 mV voltage swing, which is large enough in many cases. Moreover, with different requirements or specifications, each components can be replaced or redo the optimization.