A 16-kb 40-nm 1T1MTJ STT-MRAM Macro With Near-Memory Multiply-Accumulate Functionality and Single-Cap Offset-Canceled Sense Amplifier for Security-Aware Mobile Device

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Introduction

STT-MRAM has improved performance, higher endurance, and lower energy. However, STT-MRAM still suffers from the following challenges:

(1) Read margin is limited because the small tunnel magnetoresistance ratio (TMR)

(2) High write energy and long write latency due to large critical switching.

(3) In terms of the security, conventional logic-locking schemes with additional pins may be traced by experienced engineers.

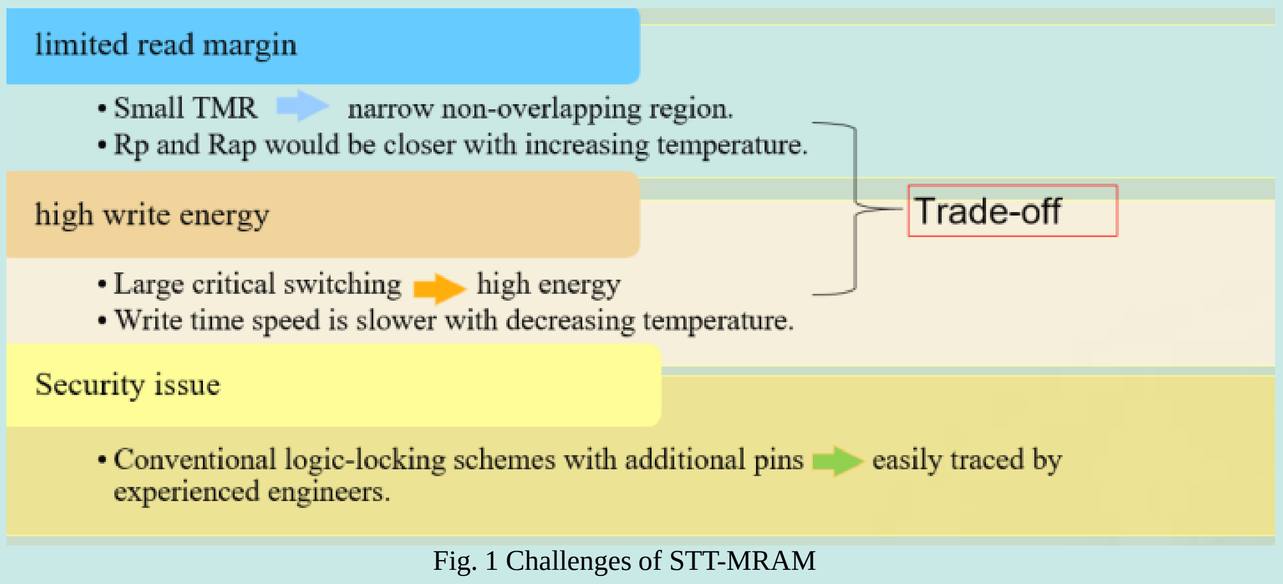


Fig. 1 Challenges of STT-MRAM

Proposed and Designed

As Fig.2, we have four proposal in this project:

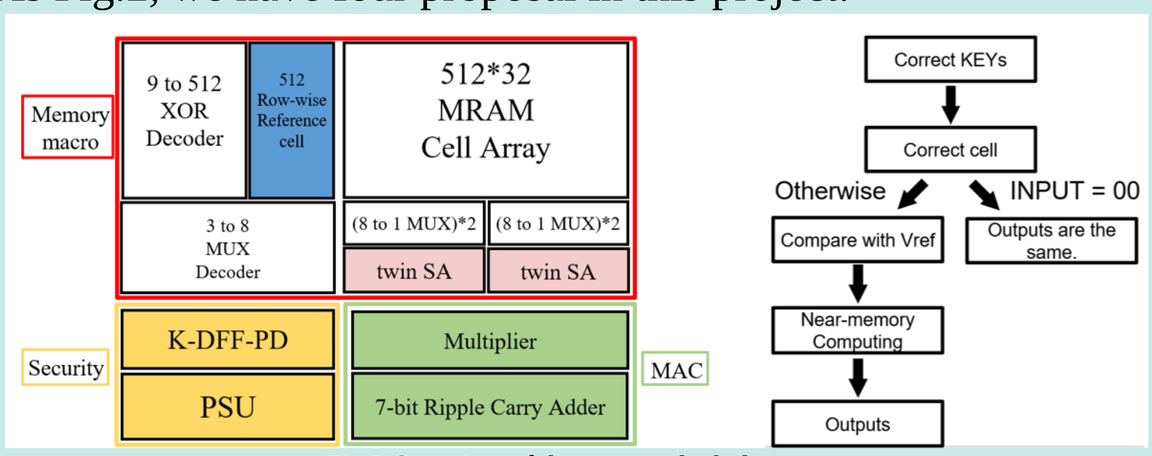


Fig.2 Overview of the proposed whole macro

(1) Self-Generated Row-Wise Reference Cell are installed on the same WL as the MRAM cell array for tracking the PVT variation in every row. Shown in Fig.3.

(2) Offset-Canceled Sensing Amplifier with single capacitor for better sensing margin, smaller area, and optimized the access-time. Shown in Fig.4.

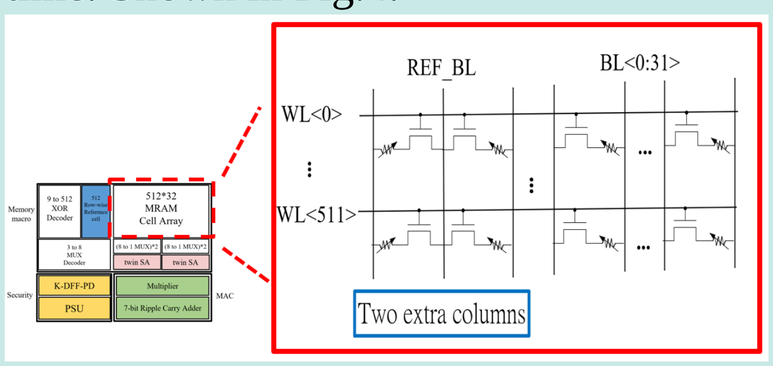


Fig. 3. 1T1MTJ MRAM array in whole macro

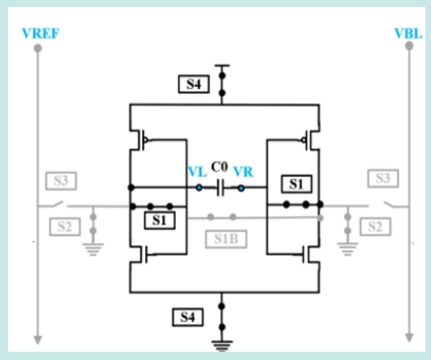


Fig. 4 Detailed of SAs

(3) Self-MAC-Termination is set after the output of the sensing amplifier, and does the calculation on 2-bit weight and 2-bit input. It can turn down the clampers, which is the discharging mechanism for BL, so the results of MAC remain the same, and the power can be saved. Shown in Fig.5.

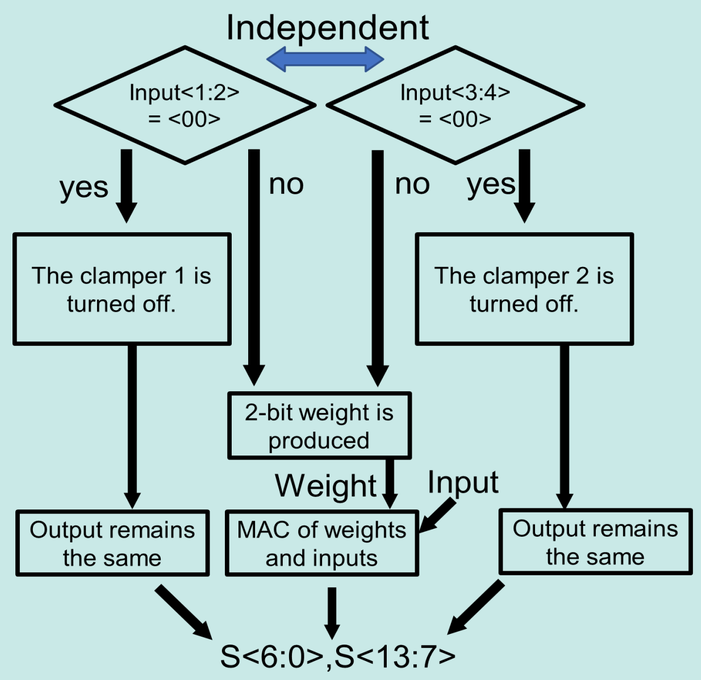


Fig. 5 The flow chart of self-MAC-termination mechanism

(4) 6T-XOR Based Memory Protector is installed before the memory macro. It contributes to select either the right or the wrong address depending on the keys the users gave. Its objective is to protect the data to be traced.

Measurement results

(1) Offset-Canceled Sensing Amplifier with Single Capacitor:

a. The offset is 50% of the conventional sensing amplifier without the function of offset canceled

b. Our work has much smaller area than the dual-cap offset-canceled sensing amplifier. Shown in Fig.6.

(2) Self-MAC-Termination: We only have 7% power consumption when the two-bits input is 00, and the probability of appearing 00 is high in reality. The average power is approximately 50% saved. Moreover, we used the ripple carry adder here so that the value can be accumulating continuously. Shown in Fig.7.

(3) 6T-XOR Based Memory Protector: It secures the data with only 2.02% area overhead. Shown in Fig.8.

(4) Measurement results of the whole circuit: The access-time achieved 2.98ns under 25℃, and get only 2.75ns when the temperature rises to 125℃. The power consumption is 0.428mW under 25℃. Moreover, the Monte analysis got 95% accuracy. Shown in Fig.9.

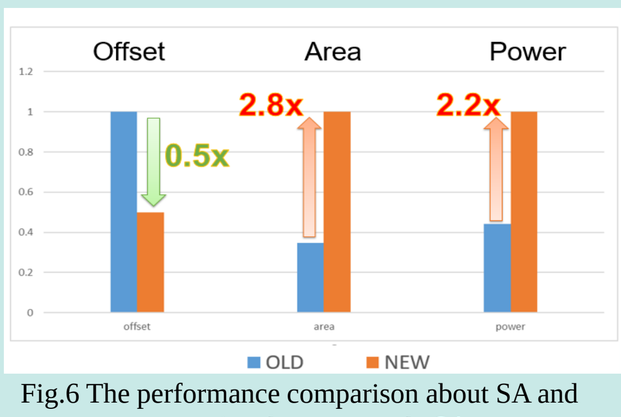


Fig.6 The performance comparison about SA and conventional cross-couple SA

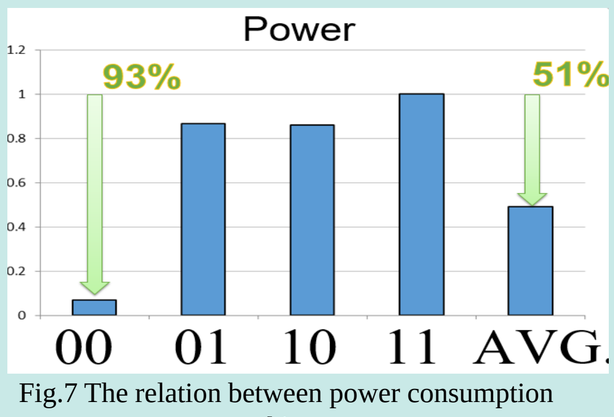


Fig.7 The relation between power consumption and input

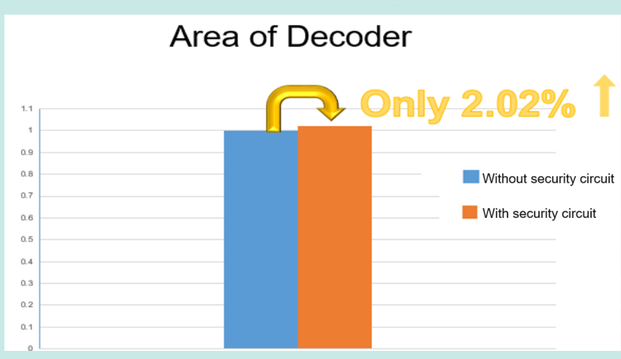


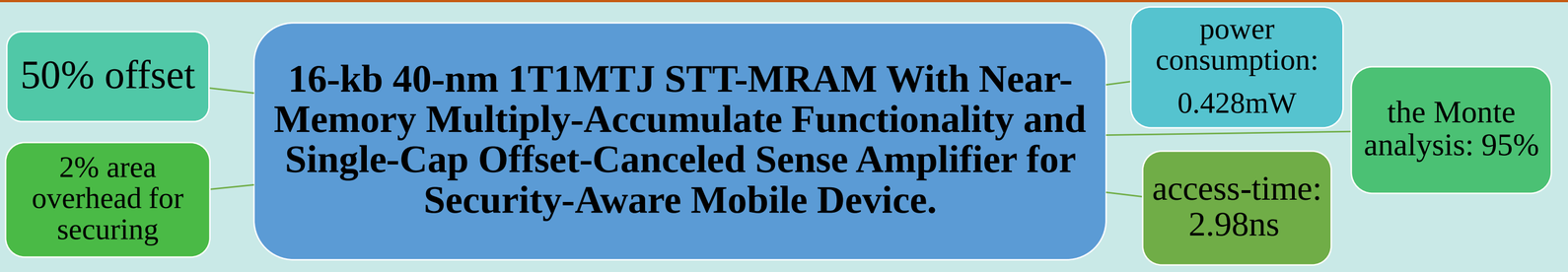
Fig.8 The decoder area comparison w/o security circuit

Temperature(℃)	25	125	-40
access time(ns)	2.98	2.75	3.18
power(mW)	0.428	0.437	0.439

Fig.9 The access time and power in different temperature

Conclusion

(1) The offset is canceled for 50%,
(2) Only 2% area overhead for protecting datas.
(3) Access-time: 2.98ns under 25℃.
(4) Power consumption is 0.428mW under 25℃.
(5) Monte analysis got 95% accuracy..



[1] Y. -C. Chiu et al., "A 22-nm 1-Mb 1024-b Read Data-Protected STT-MRAM Macro With Near-Memory Shift-and-Rotate Functionality and 42.6-GB/s Read Bandwidth for Security-Aware Mobile Device," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2021.3112182.
[2] Q. Dong et al., "A 1-Mb 28-nm 1T1MTJ STT-MRAM With Single-Cap Offset-Cancelled Sense Amplifier and In Situ Self-Write-Termination," in IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 231-239, Jan. 2019, doi: 10.1109/JSSC.2018.2872584.