A 7-bit VCO-based ADC

一個七位元基於壓控震盪器的類比數位轉換器

組別：B602　　指導教授：黃柏鈞 教授　　組員姓名：黃奐文

Introduction

A Voltage-Controlled Oscillator (VCO) based Analog-to-Digital Converter (ADC) is a novel architecture that utilizes the linear relationship between the VCO's input voltage and its output frequency for signal conversion.This project presents the design of a 7-bit VCO-based ADC. The architecture employs a highly linear VCO to linearly convert an analog voltage signal into a frequency signal. Subsequently, a counter-based Frequency-to-Digital Converter (FDC) is used to linearly transform the frequency signal into a digital code.

Architecture and Operation

Figure. (1) presents the overall architecture of this design. It contains a sample-and-hold circuit, including two transmission gate switches and two large capacitors, a linear VCO, and an FDC composed of a counter and a register, where the RST signal manages input/output sampling and counter resets.

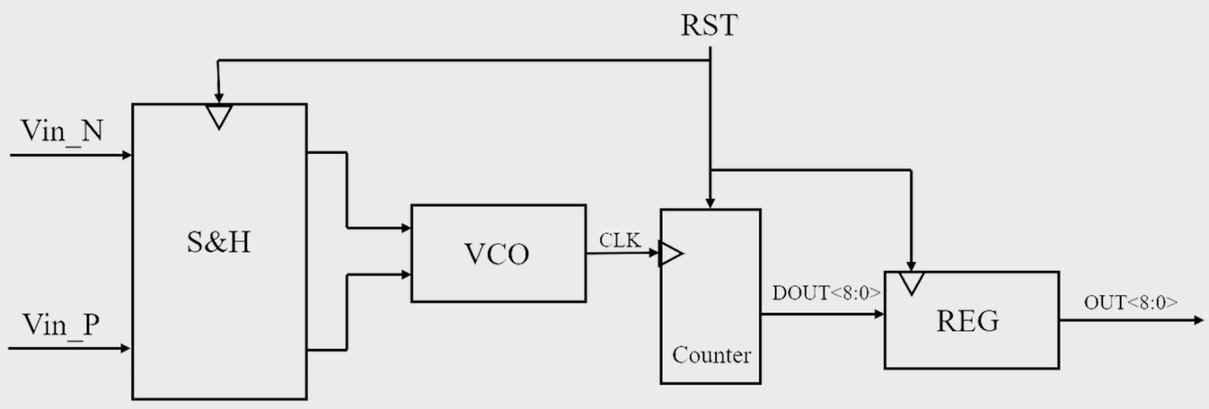

Figure. (1) Overall block diagram of the VCO_based ADC

Figure. (2) illustrates the circuit diagram of a linear VCO designed to achieve linearity through the superposition of MOS capacitors. When the control voltages Vcontn and Vcontp are increased simultaneously, the gate-to-source voltage of the NMOS decreases, while that of the PMOS increases. Consequently, the capacitance contributed by the N-type I-MOS varactor decreases, whereas the capacitance from the P-type I-MOS varactor increases. By superimposing the C-V curves generated by both varactors, the non-linear regions of the individual I-MOS varactors effectively cancel each other out, resulting in a significantly more linear overall C-V characteristic.

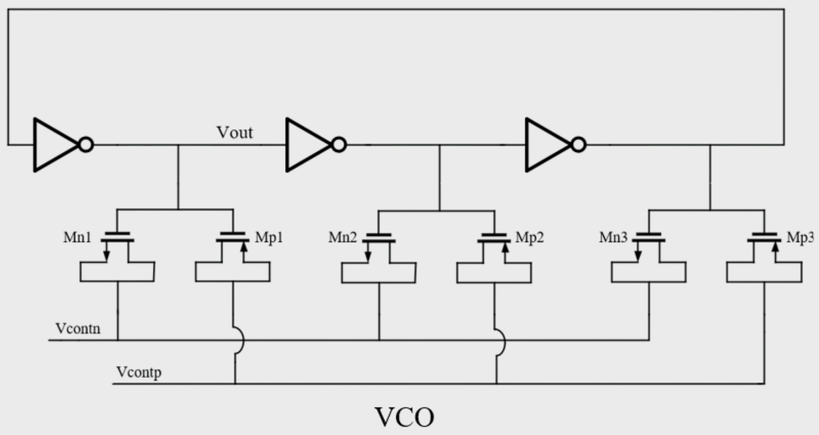

Figure. (2) Schematic of the VCO

Experimental Results

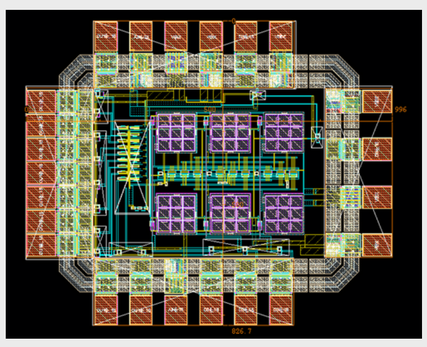

Figure. (3) The Layout

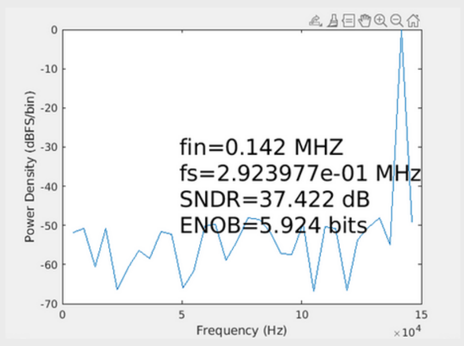

Figure. (4) Post-sim FFT spectrum

specification	Spec.	Pre-sim(tt)	Post-sim(tt)
Power Supply(V)	1.8	1.8	1.8
Power(mW)	NA	10.65	9.18
Speed (MHz)	1	0.5	0.3
Enob	7	6.196	5.924
Chip size(mm^2)	NA	0.996*0.8267	

Figure. (5) Spec and overall performance

Conclusion

This project, based on T18 process, implemented and taped-out a 7-bit VCO-based ADC. The core design achieved linearization by superimposing the C-V curves of N-type and P-type I-MOS varactors. However, the experimental results reveal that both the ENOB and the speed failed to meet the specifications.

A key trade-off was identified in the counter-based FDC architecture: increasing the ADC speed requires a wider VCO frequency range (fmax−fmin), which in turn sacrifices the VCO's linearity. This limitation resulted in a low ADC speed (< 1MHz) despite a high-frequency VCO (300-400MHz), leading to significant power inefficiency.

The chip is currently awaiting measurement. Future work should focus on improving the FDC design to better capitalize on the high sampling rate potential inherent in VCO-based architectures.

Reference

[1] S. Smith, A. Tajalli and S. -h. W. Chiang, "A VCO Linearization Technique Using Dual-VCO and Interpolation for Time-Based ADCs," 2023 IEEE 66th International Midwest Symposium on Circuits and Systems

[2] V. Nguyen, F. Schembari and R. B. Staszewski, "A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS," in IEEE Solid-State Circuits Letters, vol. 1, no. 9, pp. 190-193, Sept. 2018