國立清華大學 電機工程學系

實作專題研究成果摘要

一具放電電流的電壓時間轉換器輔以時間數位轉換器的共模電壓基底每秒兩千萬次採樣之十位元的連續漸進式類比數位轉換器

A Vcm-based 10-bit 20MS/s TDC-assisted SAR ADC with Voltage-Time Converter by Directly Discharging Current

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Abstract

Analog-to-Digital Converter (ADC) is an essential electronic component that converts analog signal into digital data, enabling analog information to be processed by digital systems. Among the various types of ADCs, one of the most widely used is the Successive Approximation Register Analog-to-Digital Converter (SAR ADC). Known for its low power consumption, medium to high resolution and relatively fast conversion speed, the SAR ADC is highly popular in a range of applications. However, as resolution increase, the constraints on the comparator become more stringent, leading to greater design complexity in SAR ADC's comparator.

Therefore, in this project, we combine SAR ADC (as the coarse part of ADC) with a Time-to-Digital Converter (TDC) (as the fine part of ADC) through Voltage-to-Time Converter (VTC) to enhance overall performance. The TDC enhances timing precision and reduces quantization errors, enabling higher resolution and more accurate digital conversion. Additionally, even as the full swing of the SAR ADC decreases, the TDC can still maintain relatively high resolution, making it highly effective in high-resolution scenarios. By incorporating the TDC, we aim to overcome challenges such as increased comparator complexity and tighter timing constraints typically associated with higher-resolution SAR ADCs.

The VTC plays a crucial role by converting the analog voltage into a time-domain signal, allowing the TDC to handle quantization in the time domain. This direct current discharge method used in the VTC not only enhances linearity but also improves tracking ability, making the design more robust for high-resolution ADC applications. This approach helps the TDC handle quantization more effectively, even as the full swing of the SAR ADC decreases, maintaining resolution while achieving better noise performance.

This project builds on the framework established in a previous master's thesis by a former lab member [1], with the design adapted from that work. The VTC architecture, chosen for its simplicity and practicality, was particularly well-suited to our design needs. While the earlier design employed a 90nm process, we transitioned to a 0.18μm process for this project. To accommodate this change, we optimized the original circuit architecture and carefully balanced performance with non-ideal factors, ensuring the design remained efficient and robust under the new process parameters.

The simulation results indicate that the proposed architecture achieves an effective number of bits (ENOB) exceeding 9.8 under a variety of corner conditions, ensuring stable performance at a sampling frequency of 20 MHz. These findings confirm the design's reliability across diverse operational environments, with the successful suppression of non-ideal effects further enhancing signal integrity and conversion precision. This makes the architecture highly suitable for high-resolution, low-power applications.

To summarize, this project introduces a coarse-fine SAR ADC design that balances high resolution and low power consumption. Through a series of optimizations and architectural improvements, the design demonstrates strong performance and stability across different process variations, as confirmed by simulation. Its efficient power usage and impressive resolution position it as a promising candidate for future applications. Nonetheless, further work could focus on increasing resolution and achieving even lower power consumption, providing a clear path for future exploration and development.

1. Introduction

The SAR ADC is a widely used ADC known for its low power consumption, compact size, and medium-to-high resolution. Its operation resembles a binary search algorithm (as illustrated in Fig. 1), where the output voltage from the Capacitive Digital-to-Analog Converter (CDAC) is iteratively compared using a comparator to determine the digital output.

The CDAC employs top-plate sampling, which helps reduce kickback noise from the comparator, improves accuracy for small signals, and enhances overall linearity. Additionally, the use of a common-mode voltage (Vcm)-based approach further improves noise immunity, enhances signal matching, and reduces offset errors, contributing to better overall performance and stability, particularly in high-precision applications, as illustrated in Fig. 2 through the voltage conversion process.

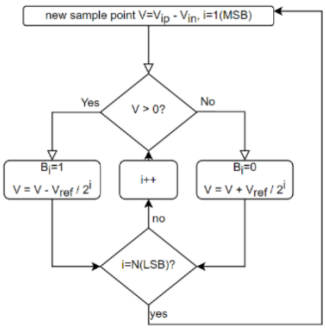
However, as the conversion resolution increases, the residual voltage on the CDAC output becomes smaller. For instance, in a 10-bit ADC, the residual voltage is reduced to around 3.5mV. This makes the mismatch and noise constraints of the comparator significantly more critical, as they must be kept below 3.5mV to ensure accurate conversion.

To alleviate the design constraints on the comparator, we utilize a Flash TDC, as referenced in [2], to handle the fine part of the ADC. The Flash TDC offers faster conversion compared to other types of TDCs, making it well-suited for this project. It is composed of delay cells, arbiters, and a Thermal-to-Binary Converter (TBC), which work together to efficiently convert time-domain signals into high-resolution digital outputs.

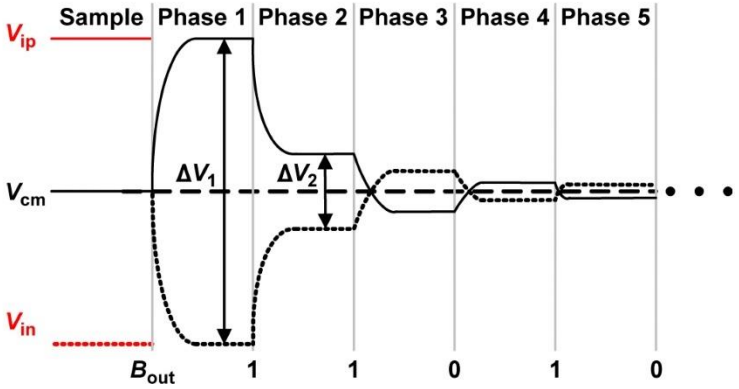
A series of delay cells and arbiters will convert the time-domain signal from the VTC into a digital domain signal encoded as thermal code. By employing a multiplexer (MUX)-based TBC, we can effectively transform the thermal code into a standard binary code that is widely used in digital systems.

The VTC uses a direct current discharge method to convert the SAR ADC's voltage-domain signal into a time-domain signal for the TDC. It discharges the residual voltage from the SAR ADC's CDAC and triggers a timing signal via a low-skewed inverter, ensuring good linearity. However, due to the time this process takes, a Flash TDC is employed for the fine conversion to enhance speed and overall performance.

Through post-layout simulation, we achieved an ENOB of over 9.8 bits with a power consumption of 1.48mW, which demonstrates the design's efficiency in balancing high resolution and low power consumption.

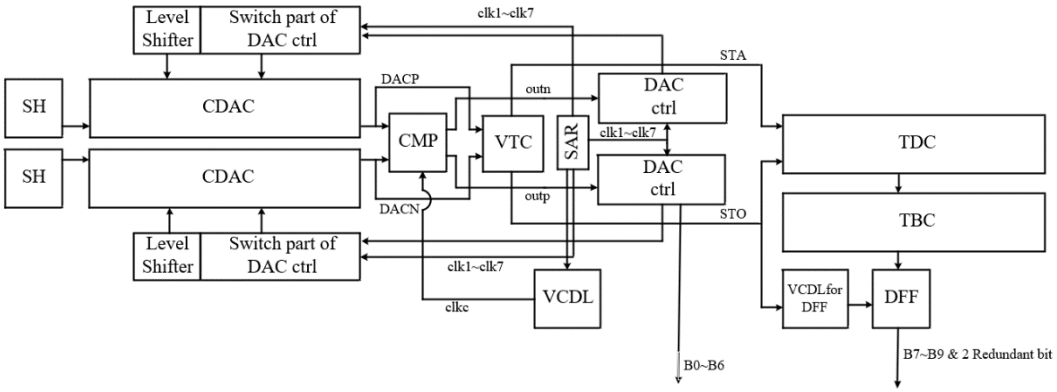


▲ Fig. 1：Flow Chart of Binary Search Algorithm for SAR ADC



▲ **Fig. 2：Voltage conversion process of Vcm-based CDAC**

2. Block diagrams and operating principles



▲ **Fig. 3：10-bit ENOB Coarse-Fine Hybrid SAR ADC Block diagram**

Fig. 3 illustrates the overall architecture of our circuit design. Initially, the differential input signal is fed into the Sample-and-Hold (S/H) circuit. When the sampling clock signal (CLK_s) is high, the S/H circuit samples the input signal. Once the CLK_s signal goes low, the S/H circuit holds the sampled signal and sends it to the P and N terminals of the comparator. The comparator then compares the voltages at these terminals and outputs the signals $Out_p$and Out_n based on the comparison results.

The signals Out_p and Out_n pass through an OR gate to generate a valid signal, which triggers the SAR logic to produce the necessary clock signals CLK_1 through CLK_7 for DAC control switching. Based on the comparator's output, Out_p and Out_n the DAC control adjusts the bottom plate voltage of the DAC capacitor array. This, in turn, causes the top plate voltage to change according to the capacitor ratio, performing capacitive voltage division. From the generation of the valid signal to the top plate voltage change constitutes one complete comparison cycle. This process repeats seven times, producing a 7-bit result, implementing the successive approximation comparison method. This 7-bit generation forms the coarse part of the design in this project.

Next, the remaining 3 bits are handled by the subsequent circuitry. After completing the 7 DAC bottom plate switches, a residual voltage remains between the top plates, referred to

as the residue voltage, which is defined as $DAC_p - DAC_n = V_{Res}$. This V_{Res} is first shifted using a level shifter, where the voltage on the p terminal of the DAC (DAC_p) is raised to ensure it remains higher than the n terminal (DAC_n). It is then converted into a corresponding time difference T_{out} through the discharge mechanism within the VTC. The T_{out} is then processed by TDC and TBC, converting it into a 5-bit digital signal. The lower-weighted 3 bits serve as the final 3 bits of the ADC result, while the higher-weighted 2 bits are treated as redundant bits. This process of generating the 3 bits and 2 redundant bits constitutes the fine conversion part of the project.

Finally, we use MATLAB code to process the 10-bit digital signal along with the 2 redundant bits. By adjusting the calibration gain, we fine-tune the overall performance to ensure that the ADC's ENOB (Effective Number of Bits) reaches the expected level. This calibration step helps optimize the final ADC accuracy and performance.

3. Simulation Results

Since our project is a hybrid ADC, there will be measurements for the coarse ADC section alone and for the combined coarse and fine ADC sections. Table 1 shows the ENOB of the coarse ADC during Pre-Sim and Post-Sim. As the coarse ADC outputs the first seven bits of the digital signal and adopts a Pure SAR ADC architecture, the specification is set at 6.9 bits, with both measurements exceeding this value.

Corner	TT	FF	SS	SF	FS
PreSim ENOB	6.9738	6.9676	6.9768	6.9744	6.9725
PostSim ENOB	6.9712	6.9642	6.9753	6.9713	6.9685

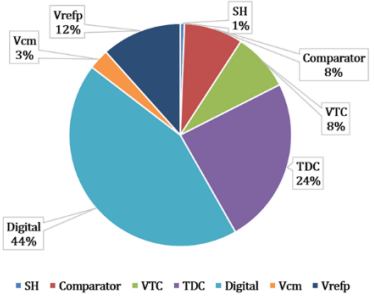
▲ Table 1：ENOB Table of Coarse ADC Part for Pre-Sim and Post-Sim

Table 2 shows the ENOB of the whole ADC during Pre-Sim and Post-Sim. The fine ADC is responsible for the remaining three bits of the digital signal while also outputting two redundant bits. As a 10-bit ADC, the ideal ENOB during both Pre-Sim and Post-Sim should reach 9.9. The designed circuit achieves the maximum ENOB specified in both simulations.

Corner	TT	FF	SS	SF	FS
PreSim ENOB	10.1356	10.3133	9.9503	10.1771	10.0952
PostSim ENOB	9.9854	10.1751	9.9081	9.9988	9.9803

▲ Table 2：ENOB Table of Overall ADC Part for Pre-Sim and Post-Sim

Power Consumption (TT Corner)



SH	9.0367(μW)
Comparator	126.10(μW)
VTC	123.83(μW)
TDC	357.06(μW)
Digital Circuit	643.92(μW)
V_{cm}	43.814(μW)
V_{refp}	171.45(μW)
Total	**1475.211(μW)**

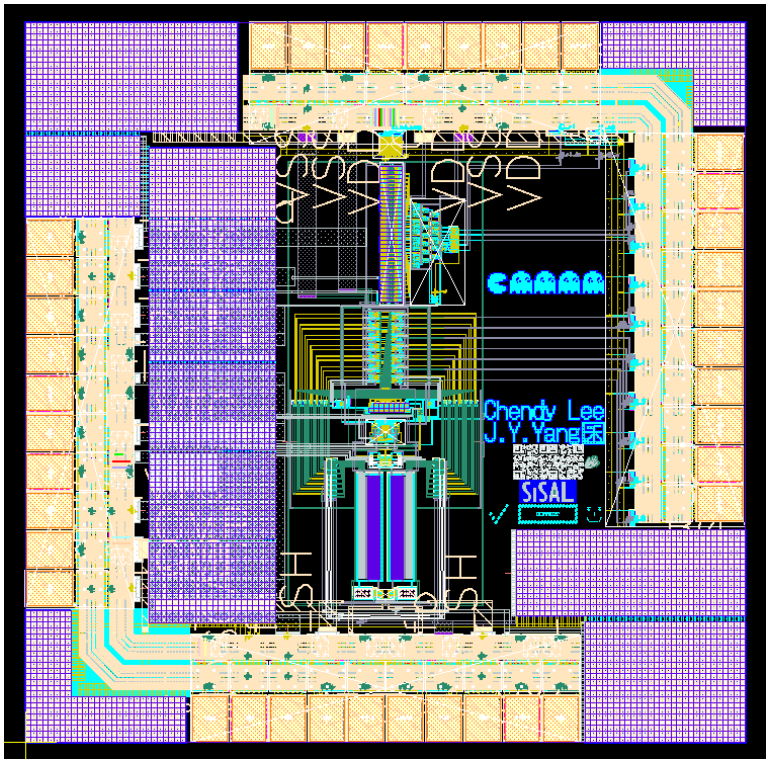
▲ Fig. 4：Power Consumption for Post-Sim (pure Core, without IO PAD)

Chip Size	$1200 \times 1200(\mu m^2)$
Transistor/Gate Count	2507
Maximum Operating Frequency	$20(MHz)$
Power Dissipation	
Total power including PAD, ESD	$3.0472(mW)$
VDD_SH	$6.7407(\mu W)$
VDD_CMP	$126.33(\mu W)$
VRefp	$185.36(\mu W)$
Vcm	$42.691(\mu W)$
VDD_VTC	$127.52(\mu W)$
VDD_TDC	$354.23(\mu W)$
VDD_Shield	$0.00191(\mu W)$
VDD_D1	$551.91(\mu W)$
VDD_D2	$103.76(\mu W)$
VDD_ED	$1548.7(\mu W)$
VDD_EA	$0.00149(\mu W)$

▲ Table 3：One period power consumption with IO PAD, including SH, Comparator, DAC, VTC, TDC, Shielding, Vcm, Digital Circuit, Digital ESD、Analog ESD。

4. Layout

Chip Size: $1200\mu m \times 1200\mu m$
Number of pins: 39



▲ Fig. 5：Full Chip Layout

5. Conclusion

In conclusion, this project demonstrates the successful implementation of a 10-bit, 20MHz Hybrid SAR ADC architecture using the T18 process. The proposed design effectively integrates a SAR ADC as the coarse ADC stage with a Time-to-Digital Converter (TDC) through a Voltage-to-Time Converter (VTC) as the fine ADC stage, thereby enhancing overall performance. By combining these elements, the architecture achieves high timing precision and reduced quantization errors, resulting in improved resolution and accuracy across different process corners.

The VTC plays a pivotal role in this design by converting the analog voltage signal into a time-domain representation. This enables the TDC to handle time-domain quantization, which is critical for maintaining high resolution even as the full swing of the SAR ADC input decreases. The use of this approach ensures robust operation and supports better noise performance, making the ADC suitable for high-resolution applications. The adoption of the T18 process in this project further reinforces the feasibility of integrating such an advanced architecture within modern semiconductor technology.

Despite the clear advantages, the project also highlights certain challenges. Notably, VTC mismatch poses a potential limitation that can impact performance. Additionally, the TDC's power consumption is relatively high due to the nature of digital operations, which could be a concern for power-sensitive applications. However, these challenges do not overshadow the overall success of the design, which demonstrates that a hybrid SAR-TDC ADC can achieve a high Effective Number of Bits (ENOB) while mitigating the complexities typically associated with comparators in higher-resolution SAR ADCs.

Ultimately, the project validates the potential of hybrid ADC architectures to address issues of comparator design complexity and strict timing constraints. By leveraging a combination of SAR and time-domain techniques, the design provides a pathway for future ADC implementations that require both high resolution and efficient performance under varying conditions.

6. References

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7. Review and reflections

楊囷曄：

在開始專題之前，雖然已經修過 VLSI、AIC 等電路設計課程，也累積了不少類比電路設計的經驗，但當面對實際下線的電路時，發現有許多我們過去未曾考慮到的實作挑戰。例如，corner 和溫度對整體電路效能的影響，以及 mismatch、noise、coupling、parasitic、混合架構前後的匹配問題等非理想效應，都對設計增加了複雜性和挑戰性，使得每個細節都必須謹慎考量。

此外，這是我第一次接觸完整的類比電路設計流程（Full Custom Design Flow）。在開始畫整體電路的 layout 之前，需要進行許多子電路的模擬，並使用 behavior model 來預估電路的運行情況，這讓我對電路中的 mismatch 和 noise 規範有了更清楚的定義和要求。畫 layout 的過程中，我也學習了許多以前不曾接觸過的細節和技巧，例如使用 Guard ring 和 VDD Shielding 來防止 coupling 和 noise 的干擾，以及如何利用 MOSCAP 來維持外部定電壓的穩定性並提供額外的 density 以消除 DRC 錯誤。此外，還學會了 I/O PAD 的擺放方式、選用合適的 PAD 類型以及走線的技巧。

在過去幾個月裡，從文獻回顧到最終的電路下線，我學習到了很多寶貴的知識，並在類比電路設計實作中獲得了豐富的經驗。特別感謝我的隊友李全棣在這段期間的協助與分工合作，他的專業知識幫助了我很多；也感謝實驗室的學長姐在研究之餘抽出時間為我們解答疑惑，幫助我們解決實作中的各種困難與挑戰。最後，感謝教授設計了這麼扎實且知識含量豐富的專題訓練，並在每次會議中給予我們指導與建議，幫助我發現過程中的盲點。這次完整的 Full Custom Design Flow 經驗，使我的實作能力有了顯著提升。

李全棣：

這次專題讓我第一次真正體驗到從頭到尾的完整 Full Custom Design Flow。從文獻回顧、前期規劃到最終下線，每個環節都充滿挑戰，也大幅拓展了我對電路設計的理解。在實作的過程中，我深刻體會到理論與實際之間的差距。例如，當進行設計時，必須面對許多非理想效應的影響，包括 mismatch、noise、parasitic 等等不理想效應，我們

在實作上會遇到這些問題，我們便要學會利用電子學的概念來分析這些不理想效應，並想辦法如何去改善和解決它們。 這次專題也是我第一次使用 TSRI 的資源進行電路模擬與晶片布局設定。在開始畫整體電路 Layout 之前，我們這組花了許多時間進行 Sub Circuit 的模擬，並透過 Behavior model 來預估電路運行的情況，這讓我對 mismatch 和 noise 等規範有了更明確的理解。在 layout 過程中，我學會了如何利用圍 Guard ring 和 VDD Shielding 來減少干擾，並透過 MOSCAP 維持外部電壓的穩定性，同時解決 DRC 錯誤。 這次專題能夠順利完成，首先我要感謝我們的指導教授，謝志成老師，他在 Major Meeting 上的教導與建議；並同時感謝陳冠呈、黃昱翔學長，在 Minor Meeting 上進度驗收與糾正。同時感謝，專題指導學長，游智鈞和陳柏澖，一路來的栽培與資源供給。最後我要感謝我的隊友，楊困曄同學，他在這次 PostSim 與 Layout 貢獻了很多心力，才可以讓我們的晶片能夠成功送出去給 TSRI 下線。我希望未來直升研究所後，將這次專題中學到的理論與技術應用到日後的研究中。