A Vcm-based 10-bit 20MS/s TDC-assisted SAR ADC with Voltage-Time Converter by Directly Discharging Current

一具放電電流的電壓時間轉換器輔以時間數位轉換器的共模電壓基底

每秒兩千萬次採樣之十位元的循序漸進式類比數位轉換器

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Abstract

Analog-to-Digital Converters (ADCs) are crucial for converting analog signals into digital data, with the Successive Approximation Register ADC (SAR ADC) being especially popular due to its low power, moderate-to-high resolution, and fast conversion. However, as resolution demands increase, the design complexity of the SAR ADC comparator also grows due to tighter constraints.

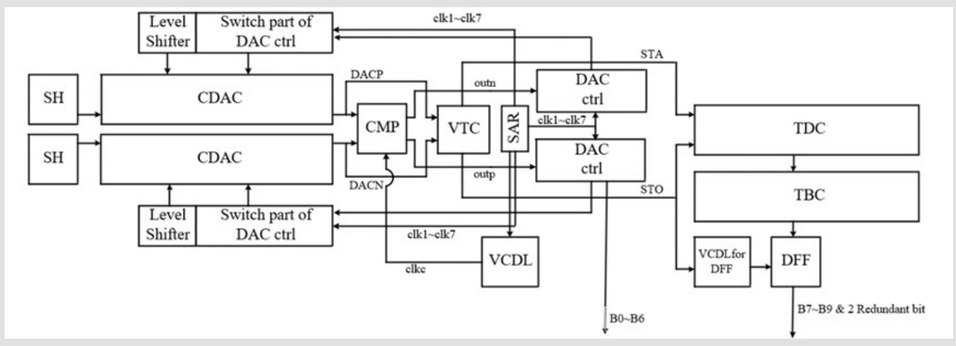
This project enhances SAR ADC performance by integrating it with a Time-to-Digital Converter (TDC) via a Voltage-to-Time Converter (VTC). The TDC improves timing precision and minimizes quantization errors, enabling higher resolution and more accurate digital conversion. Even as the SAR ADC's full swing decreases, the TDC maintains high resolution, effectively addressing comparator complexity and timing challenges typically associated with high-resolution SAR ADCs.

Circuit Structure

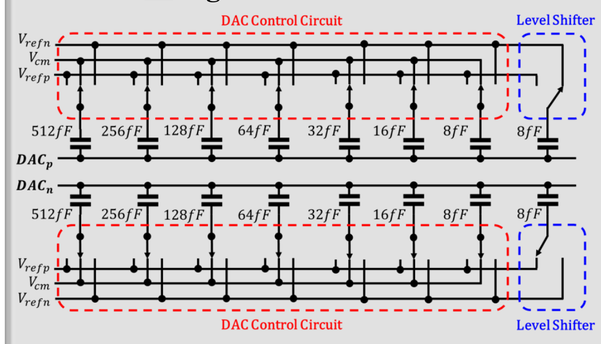
Fig. 1 illustrates the circuit's architecture. The differential input signal is first processed by a Sample-and-Hold (S/H) circuit, which samples the signal when the clock is high and holds it as it goes low, delivering the signal to the comparator's P and N terminals. The sampling mechanism employed is top plate sampling, with the CDAC architecture depicted in Fig. 2. During the sampling phase, the differential input signal is stored on the top plate of the CDAC. When the conversion begins, the comparator directly compares the differential signal at the start of the first conversion cycle. Compared to bottom plate sampling, this approach eliminates the need for one additional conversion step, reduces the size of the largest capacitor for the same unit capacitor size, and thereby saves both area and conversion time. The complete waveform of the top plate voltage during conversion is shown in Fig. 3.

Once the comparator evaluates the terminal voltages, its output is processed by an OR gate to generate a valid signal. This signal triggers the SAR logic, which produces clock signals to control the DAC. The DAC adjusts the bottom plate voltage of the capacitor array, causing the top plate voltage to change dynamically based on the capacitor ratios, thereby achieving voltage division. This 7-step comparison process produces a 7-bit result, constituting the coarse conversion stage.

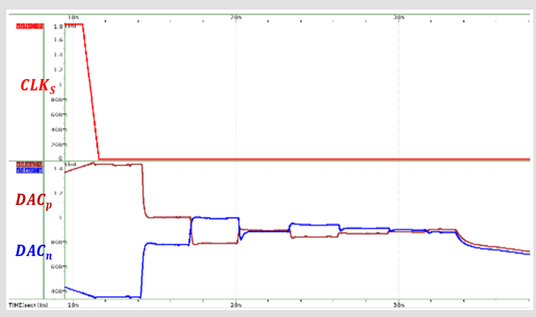
The remaining 3 bits are generated by subsequent circuitry. Following the 7 DAC adjustments, a residual top plate voltage, or residue voltage, is processed by a level shifter, which raises the DAC's p-terminal voltage to ensure it remains higher than the n-terminal for accurate conversion. The level-shifted signal is then converted to a time difference through the VTC discharge mechanism. The TDC and TBC then convert this time difference into a 5-bit digital signal, where the lowest 3 bits serve as the final ADC bits and the highest 2 as redundant bits. Finally, MATLAB processes the 10-bit signal and 2 redundant bits to calibrate the gain and optimize ENOB (Effective Number of Bits) for enhanced ADC accuracy and performance.



▲ Fig. 1: 10-bit ENOB Coarse-Fine Hybrid SAR ADC Block diagram



▲ Fig. 2: Top-plate sampling CDAC and Level Shifter



▲ Fig. 3: Post-sim waveform of Top plate

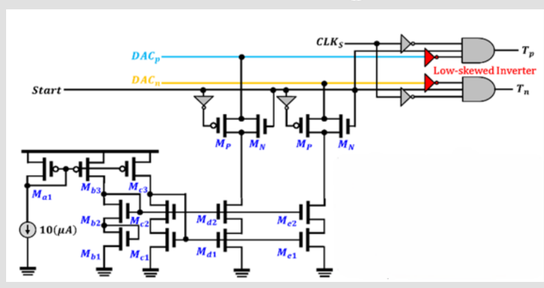
Hybrid Architecture

This hybrid ADC architecture features a standard Vcm-based SAR ADC as the Coarse ADC, performing an initial 7-bit conversion. The Fine ADC then processes the residual signal to achieve higher precision. Once the Coarse ADC completes its comparison, the VTC (Fig. 4) begins operation, using clk7 to activate a transmission gate that discharges the top plate through a current mirror.

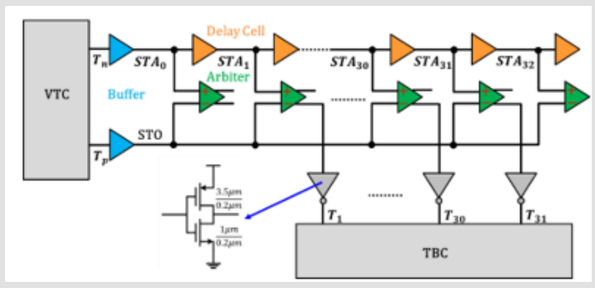
As the DAC terminals discharge, output signals STA and STO are generated when threshold voltages are reached. The timing difference between these signals represents the residual voltage from the Coarse ADC, as illustrated in the waveform in Fig. 5.

To enhance accuracy, the VTC employs a linear transmission gate and a wide-swing cascode current mirror to ensure MOS devices remain in saturation and enable stable current replication. A bias circuit provides the required voltages, while a P-type current mirror maintains a current ratio of 1:1:2 between the current mirror and bias circuits.

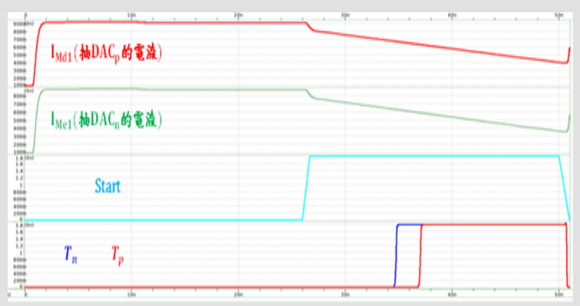
The Fine ADC's TDC (Fig. 6) converts the VTC output into a thermal code, which is processed by the TBC to produce the final binary output. The TDC includes 33 delay cells and arbiters to detect timing differences between the STAi and STO signals, generating a thermal code with sequential "1s" followed by "0s." This code is then translated by the TBC into a 3-bit fine result, significantly improving the resolution and accuracy of the hybrid ADC. The TDC operation waveform is shown in Fig. 7.



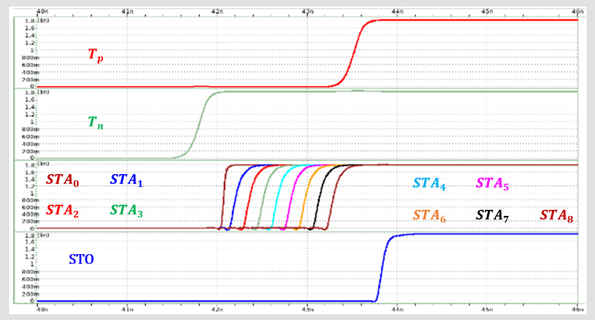
▲ Fig. 4: Schematic of VTC



▲ Fig. 6: Schematic of TDC



▲ Fig. 5: Post-sim waveform of VTC



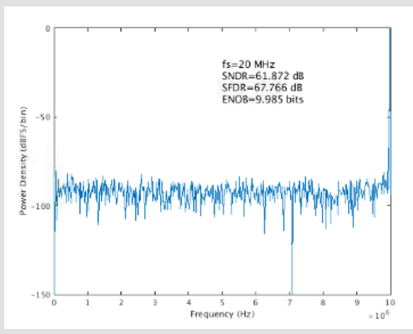
▲ Fig. 7: Post-sim waveform of TDC

Simulation Results

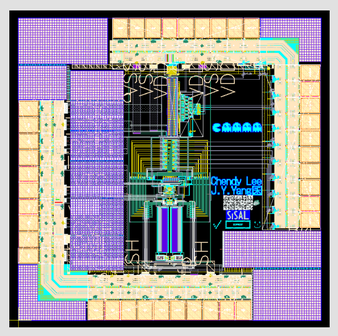
Table 1 shows the ENOB results for the Hybrid SAR ADC at each process corner, both in Pre-sim and Post-sim, under conditions of 25°C, a sampling rate of 20MHz, and an input signal frequency of 10MHz (Nyquist Frequency). Fig. 8 presents the FFT analysis of the output data (Post-sim at the TT corner, 25°C), and Fig. 9 illustrates the layout of the entire chip.

Corner	Pre-sim	Post-sim
TT	10.1356	9.9854
FF	10.3133	10.1751
SS	9.9503	9.9081
FS	10.0952	9.9803
SF	10.1771	9.9988

▲ Table 1: Pre-sim & Post-sim ENOB measure results



▲ Fig. 8: FFT analysis of the output data



▲ Fig. 9: Layout of the entire chip

Conclusion

This project successfully demonstrates a 10-bit, 20MHz Hybrid SAR ADC architecture using T18 process, combining SAR ADC as the coarse ADC with TDC via VTC as the fine ADC to enhance overall performance. This hybrid approach achieves high timing precision and reduced quantization errors, resulting in improved resolution and accuracy across various process corners. The VTC effectively converts the analog voltage to a time-domain signal, allowing for time-domain quantization by the TDC, which enables robust resolution even with reduced SAR ADC input swing. Though challenges like VTC mismatch and higher TDC power consumption due to digital operations remain, the design meets performance goals and validates the potential of a hybrid SAR-TDC ADC to maintain high ENOB with reduced comparator complexity and timing constraints.

References

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