Design of a 5 V-to-3.3 V Fast-Transient Flipped-Voltage-Follower LDO for GaN Gate Driver Applications

Group Number: A650 **Advisor: Prof. Wong, Roy King-Yuen** **Members: Hu, Jia-Wei**

Introduction

In GaN gate driver applications, the internal supply voltage must remain stable during high-speed switching. However, rapid load-current variation and input ripple may cause output overshoot, undershoot, and ringing in the LDO supply. Therefore, this project adopts a 5 V-to-3.3 V FVF-based LDO with a fast local feedback path to improve transient recovery and reduce output voltage fluctuation.

Design Challenges

- High-speed switching in GaN gate drivers causes rapid load-current variation
- Slow feedback response leads to overshoot, undershoot, and ringing
- Input ripple and switching noise degrade output stability and PSRR
- Limited supply energy may cause input voltage droop and affect regulation

Design Specifications

- Load condition: 10 pF || 5 kΩ
- Load-current step: 400 μA ↔ 800 μA
- Target output ripple: ~10 mV
- Target PSRR: ~32 dB

Research Methodology

- Adopt FVF LDO architecture for fast local feedback
- Implement and simulate the circuit in Cadence Virtuoso
- Perform transient & AC simulations to evaluate response and PSRR
- Sweep for parameter optimization
- Analyze output ringing, overshoot, and recovery behavior

Design Optimization & Simulation Results

Architecture Selection

This is a dual-loop FVF LDO architecture that combines a global error-amplifier loop 2 with a local fast-feedback loop 1. The local loop directly controls the pass transistor and rapidly suppresses output-voltage disturbance, resulting in faster transient recovery and improved stability under small output-capacitance conditions.

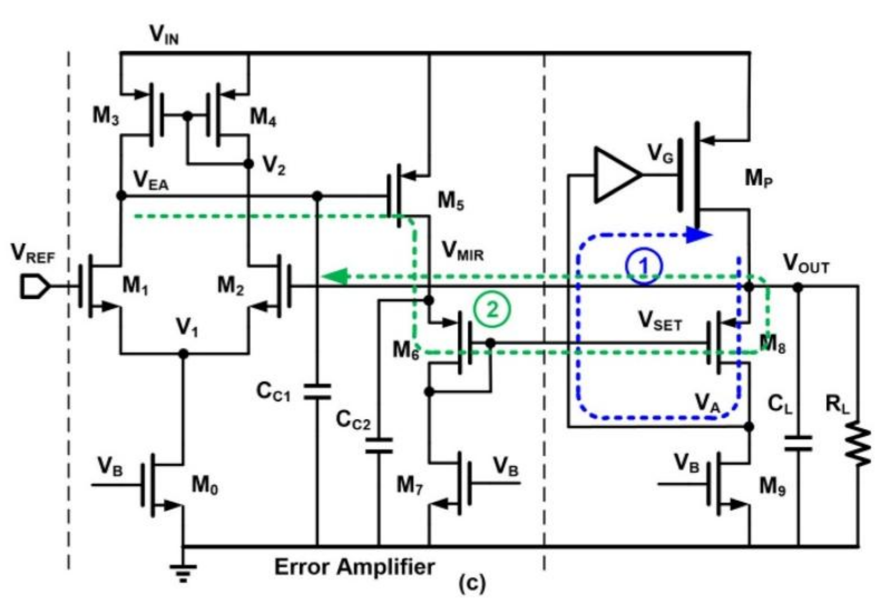

Fig.1 Reference architecture of the Example-3 FVF LDO with fast local feedback loop. Adapted from [1]

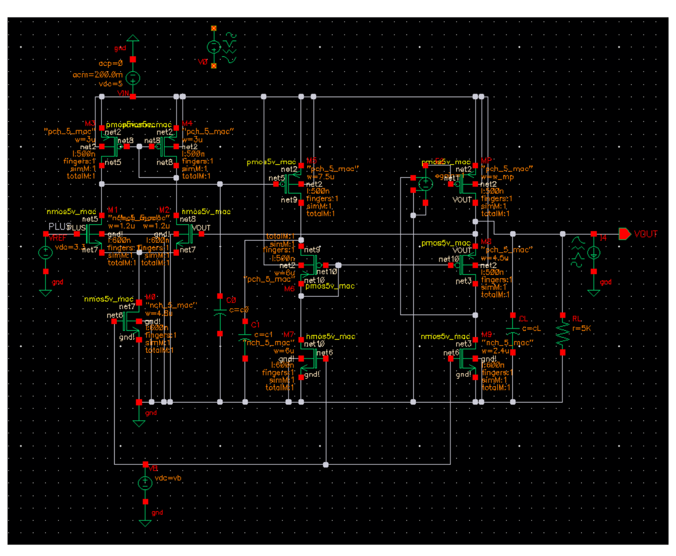

Fig.2 Schematic and simulation testbench of the proposed FVF LDO

Parameter Optimization Results

The compensation capacitors and pass transistor width were swept. C0 = 20 pF provides a more stable transient response, while increasing C1 does not effectively reduce output ringing, so C1 = 0 pF is selected. In addition, increasing the pass transistor width enhances current-driving capability. When WMP increases from 4 μm to 8 μm, the output ringing amplitude is reduced from about 0.23 V to 0.075 V. Therefore, WMP = 8 μm is chosen as the final design parameter.

Device	W/L (μm)
M0	4.8 / 0.6
M1	1.2 / 0.6
M2	1.2 / 0.6
M3	3 / 0.5
M4	3 / 0.5
M5	7.5 / 0.5
M6	6 / 0.5
M7	8 / 0.8
M8	4.6 / 0.5
M9	2.4 / 0.6
MP	8 / 0.5

Table 1 Final selected Transistor sizing of the proposed FVF LDO

Device	Value
CL	10 pF
RL	5 kΩ
C0	20 pF
C1	0 pF

Table 2 Final selected Passive component values of the proposed FVF LDO

Simulation Results

A 0.2 V, 100 kHz sinusoidal ripple was applied at the input. The output voltage varied between 3.2698 V and 3.3315 V, corresponding to 61.7 mV peak-to-peak ripple. This translates to an output amplitude of approximately 30.9 mV, resulting in an estimated PSRR of about 16.2 dB at 100 kHz.

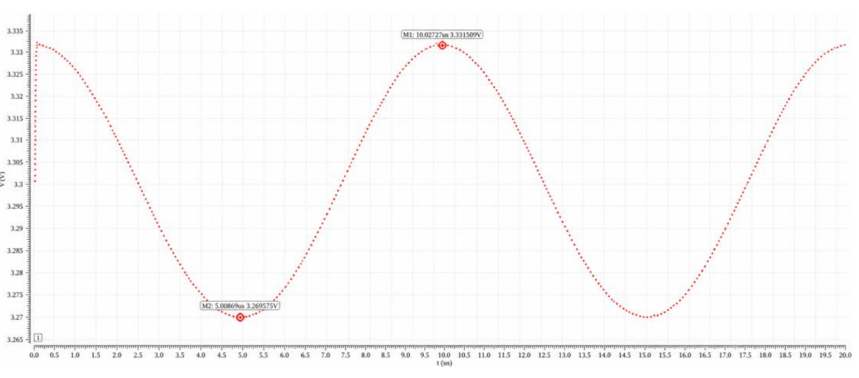

Fig.3 Output ripple response under 0.2 V, 100 kHz input ripple

The ripple transfer magnitude remains small at low frequency and increases rapidly at high frequency. This indicates that the regulator provides better low-frequency rejection, while PSRR degrades at higher frequencies due to bandwidth limitations.

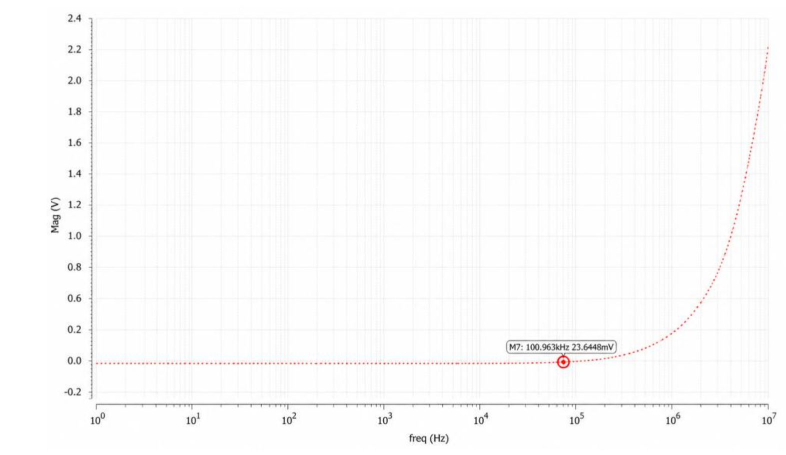

Fig.4 AC response with 0.2 V input AC magnitude from 1 Hz to 10 MHz

Under 400 μA–800 μA load-current switching, the output voltage momentarily deviates from the 3.30 V nominal value, with undershoot to 3.237 V and overshoot to 3.348 V, before returning to steady state. The zoomed transient waveform shows a peak overshoot of about 3.348 V after the load step. The output recovers close to 3.30 V within 0.5 μs.

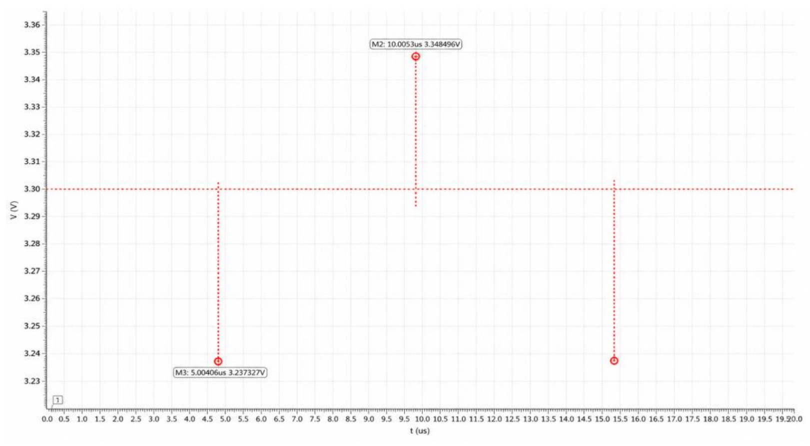

Fig.5 Full 20 μs load transient response under 400 μA–800 μA current switching

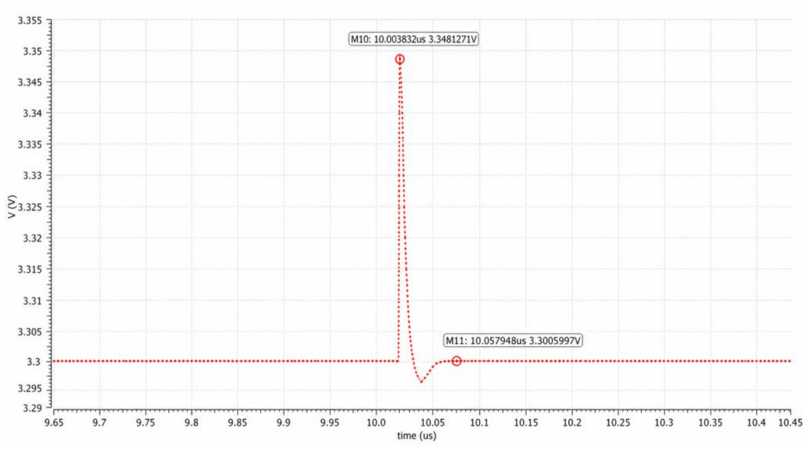

Fig.6 Zoomed load transient response around the switching event

Conclusion

- Under 400 μA–800 μA load-current switching, the output returned close to 3.30 V with a maximum overshoot of about 3.35 V, corresponding to about 50 mV deviation and 1.5% output error.
- The optimized design achieved a recovery time of about 0.5 μs, showing fast transient response under the target load condition.
- In the 100 kHz input-ripple test, the output ripple was about 61.7 mV, corresponding to an estimated PSRR of about 16.2 dB.
- Future work includes PSRR enhancement, stability analysis, corner simulation, verification under different load conditions, and integration into the full GaN gate driver system.

[1] G. Cai, Y. Lu, C. Zhan, and R. P. Martins, "A fully integrated FVF LDO with enhanced full-spectrum power supply rejection," IEEE Trans. Power Electron., vol. 36, no. 4, Apr. 2021, doi: 10.1109/TPEL.2020.3024595.
[2] R. G. Carvajal et al., "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 7, Jul. 2005.
[3] N. Liu, B. Johnson, V. Nadig, and D. Chen, "A transient-enhanced fully-integrated LDO regulator for SoC application," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2018.
[4] T. Chien, C. Chen, S. Li, and C. Tsai, "A fast transient flip voltage follower based low dropout regulator with AC-coupled pseudo tri-loop technique without using any output capacitor," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Mar. 2019.
[5] Texas Instruments, "UCC27611 5-V, 4-A to 6-A low side GaN driver," UCC27611 Datasheet, SLUSBA5F, Dec. 2012, revised Mar. 2018.