Time-Based Digital LDO Regulator with Fractionally Controlled Power Transistor Strength and Fast Transient Response

具快速暫態反應的時機基底數位低壓降穩壓器

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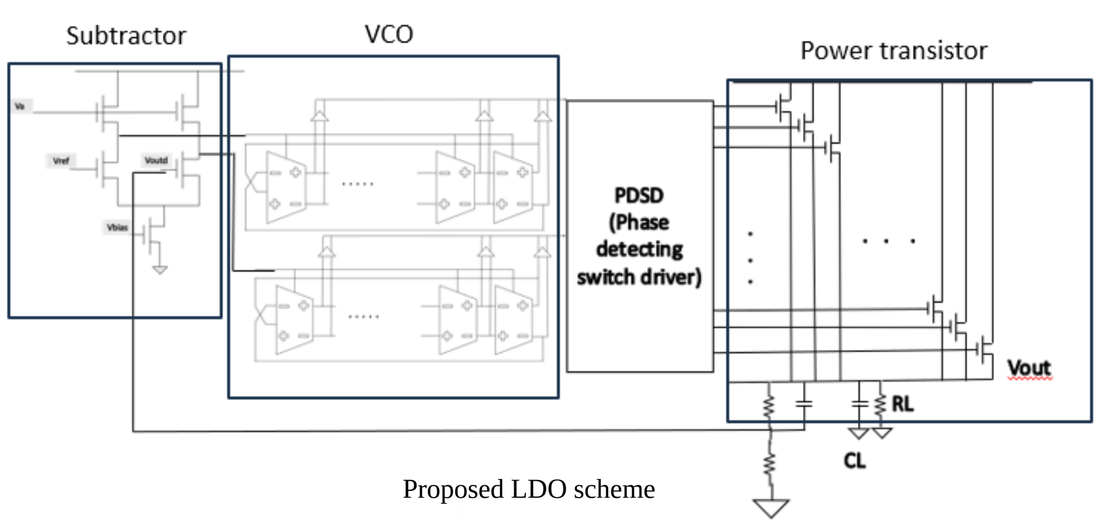
Abstract

Digital low-dropout regulators have gained more favor among designers compared to traditional analog ones due to their scalability and ease of frequency compensation. However, the drawback of Digital LDOs lies in their dependence on the internal clock frequency. Since the output voltage is compared with the reference voltage only once per clock cycle, the transient response speed is limited. Although increasing the clock frequency can enhance the transient response, this approach significantly increases the circuit's power consumption.

Therefore, this project aims to improve the transient response speed of Digital LDOs while maintaining high power efficiency. Our project focuses on designing a Digital LDO with fast transient response. The design consists of three blocks: a Subtractor, a voltage-controlled oscillator , and a phase-detecting switch driver (PDSD). The Subtractor generates a control voltage that is highly sensitive to changes in the system output, which in turn controls the oscillation frequency of the VCO, This is the key to improving the transient response speed.. The VCO's output serves as the clock input to the PDSD, and the PDSD output controls the on/off state of the power transistor. This approach achieves a fixed phase difference, minimizing output ripple and ensuring stable regulation.

Proposed Scheme



Proposed LDO scheme

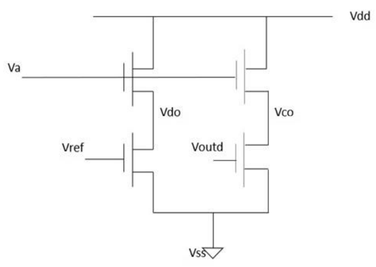
The principle of this system lies in using the Subtractor's output to control the oscillation frequency of two 32-stage voltage-controlled oscillators (VCOs). When there is a difference between V_{outd} and V_{ref} , the outputs of the two VCOs at the same stage will produce a phase difference.

The outputs of the two 32-stage VCOs are fed into the Phase Detecting Switch Driver (PDSD) as inputs. The PDSD then outputs the phase difference between the two, which is used to control the on-time of the power transistors. When $V_{outd} > V_{ref}$, the on-time of the power transistors is reduced; when $V_{outd} < V_{ref}$, the on-time is increased. This mechanism establishes a negative feedback loop for the entire system.

In the system's steady state, the phase difference remains fixed, and the number of power transistors switching simultaneously is either 0 or 1. This minimizes the output voltage ripple.

Sub Blocks

Subtractor

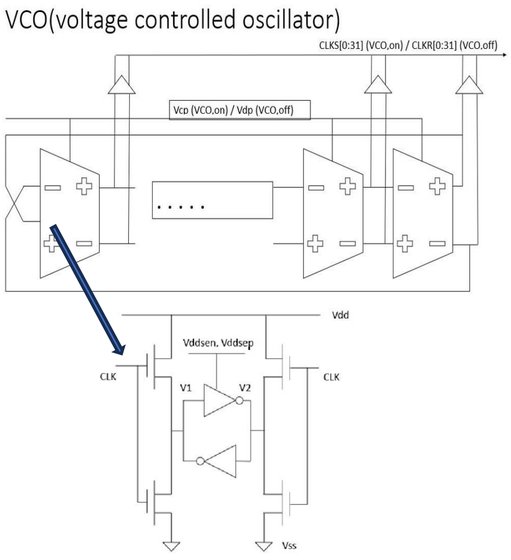


The voltage output $V_{co} \propto V_{ref} - V_{outd}$ controls VCO_{ON} ,While $V_{do} \propto V_{outd} - V_{ref}$ controls VCO_{OFF} .

This difference makes phase difference exists between VCO'_{ON}s and $VCO'_{OFF}s$ output

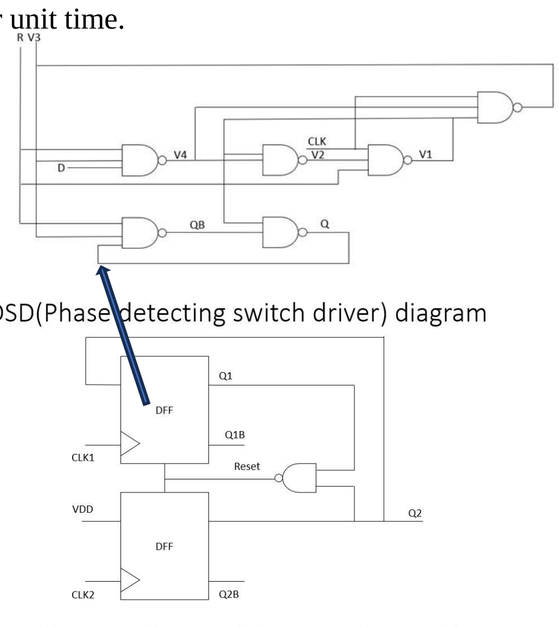
Phase difference $\Phi_{ERR} = \Phi_{VCOON} - \Phi_{VCOOFF}$

VCO(voltage controlled oscillator)

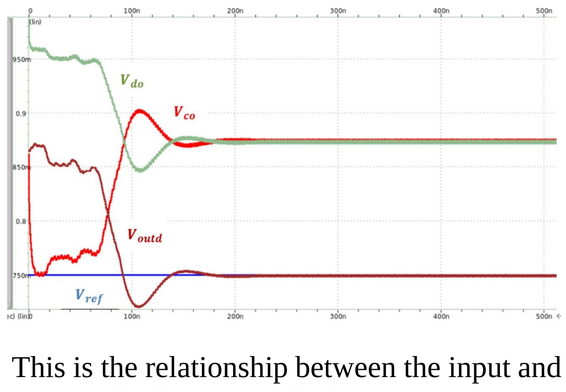


The outputs V_{co} and V_{do} from the Subtractor are used as V_{dd} for the 16-stage voltage-controlled oscillators VCO_{ON} VCO_{OFF} , respectively. The oscillation frequency of each VCO is proportional to its V_{dd}.

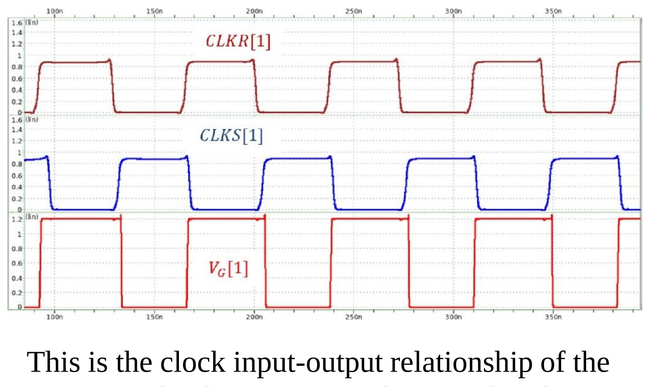
The difference V_{co} and V_{do} generates a phase difference $\Phi_{ERR} = \alpha \times \frac{2\pi}{32}$, where α represents the number of power transistors simultaneously turned on. When α is not an integer, it signifies the average number of transistors turned on per unit time.



The same-stage outputs, CLKS[K] and CLKS[R], generated by VCO_{ON} and VCO_{OFF} , respectively, are used as the clock inputs for the upper and lower D flip-flops (DFFs). The rising edge of CLKS[K] causes the PDSD output V_g to drop to V_{ss} , whereas the rising edge of CLKS[R] causes V_g to rise to V_{dd} . This mechanism controls the on-time of the connected PMOS power transistor during a single clock cycle.

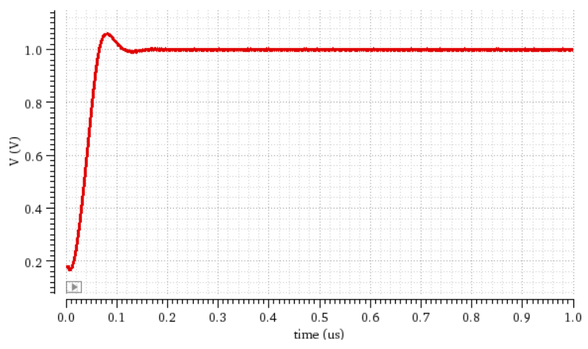


This is the relationship between the input and output of a Subtractor. In the picture, we can see that $V_{co} \propto V_{ref} - V_{outd}$ and $V_{do} \propto V_{outd} - V_{ref}$

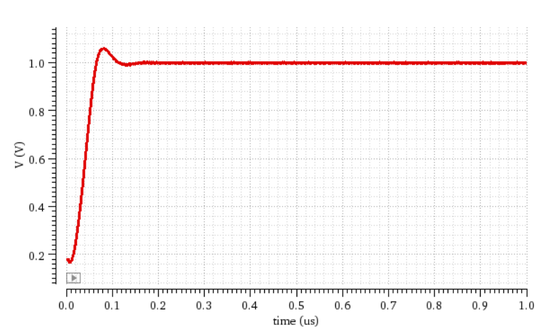


This is the clock input-output relationship of the PDSD. In the diagram, it can be seen that the rising edge of CLKS[1] will cause the output Vg[1] of the PDSD to drop to V_{ss}; on the other hand, the rising edge of CLKR[1] will cause Vg[1] to rise to V_{dd}.

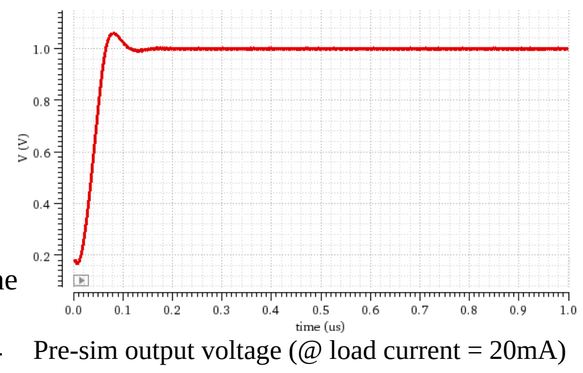
Simulation Results



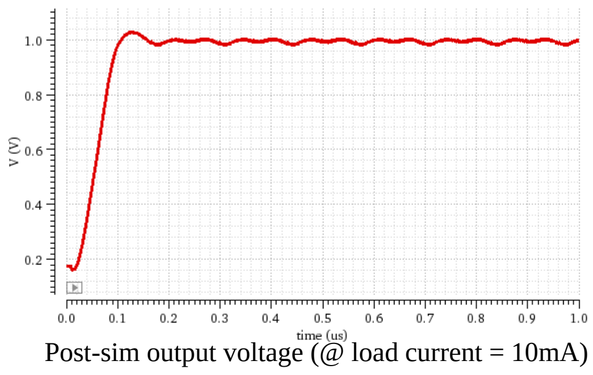
Pre-sim output voltage (@ load current = 3.33mA)



Pre-sim output voltage (@ load current = 10mA)



Pre-sim output voltage (@ load current = 20mA)

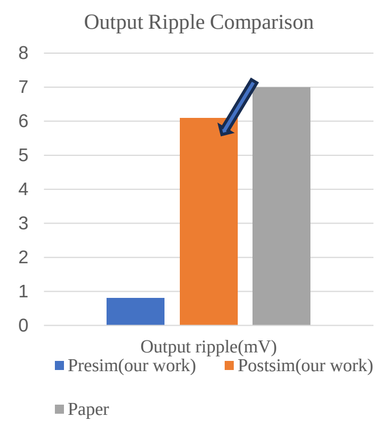


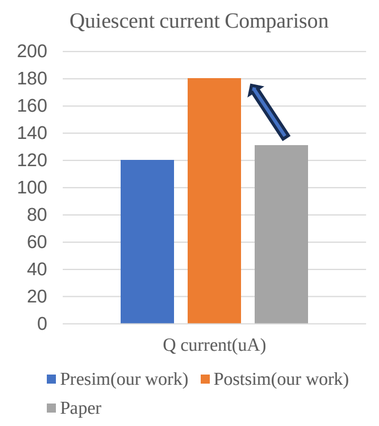
Post-sim output voltage (@ load current = 10mA)

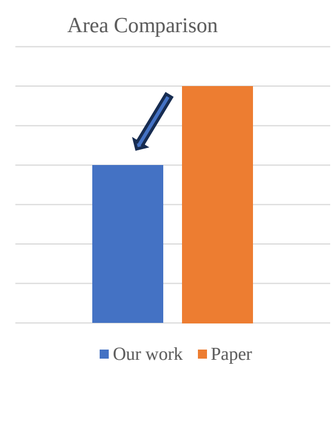
In pre-sim, under the condition where the load current varies from 3 mA to 20 mA, the system maintains stable operation with $Vout$ locked nearby 1 V; however, it cannot sustain stability beyond this range.

Additionally, we tested the system under five different corners and observed stable operation across a temperature range of 10°C to 40°C. At TT corner 25°C, output voltage ripple = 0.8 mV, quiescent current =120.31 μA, and transient response time = 124.21 ns. In the post-sim results ,We evaluated the system's performance at the TT corner and 25°C. Apart from confirming the system's stability, we measured output voltage ripple = 6.1 mV, quiescent current = 180.43 μA, and transient response time = 191.77 ns. In comparison to paper [1], the voltage output ripple is 7mV in steady state, with 131μA quiescent current and the settling time is 80 ns with transient detector but about 400ns without transient detector.

Comparison with the paper

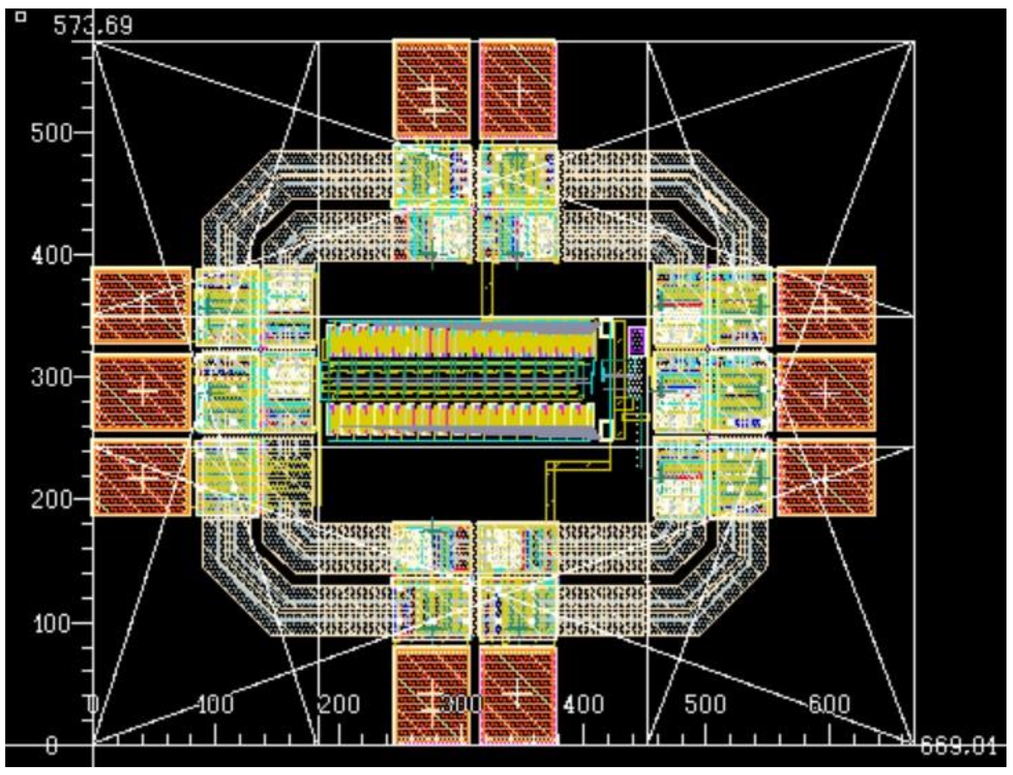






When compared to the configuration in the original paper without the transient detector, our design demonstrates superior settling time, with no significant decrease in quiescent current and power efficiency. Additionally, our output ripple in presim and postsim are all better than the 7mV reported in the original paper. Also, without transient detector, our layout area is also smaller than the original work.

Layout



[1] Jin-Gyu Kang, Min-Gyu Jeong, and Jeongpyo Park, and Changsik Yoo Department of Electronic Engineering Hanyang University, Seoul, Korea, Time-Based Digital LDO Regualtor with Fractionally Controlled Power Transistor Strength and Fast Transient Response, IEEE Asian Solid-State Circuits Conference November 4 – 6, 2019 [2] D. Kim, et al., "A 0.5V-VIN 1.44mA class event-driven digital LDO with a fully integrated 100pF output capacitor," Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf. pp. 346-348, 2017.

[3] S. Kundu, et al., "A fully integrated 40pF output capacitor beat- frequency-quantizer-based digital LDO with built-in adaptive sampling and active voltage positioning," Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf. pp. 308-309, 2018.