SONOS 快閃式記憶體操作區間之結構變化模擬分析

TCAD Simulation of Operation Windows for Critical Structures in SONOS Flash Memory Device

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ABSTRACT

Recently, with the development of portable electrical product, the non-volatile memory device has more and more indispensable in our daily life with the help of advancing structure, technology, and the reliability of the operation condition. Especially the SONOS flash memory device, which structure is stacked on silicon-oxide-nitride-oxide-silicon. Using Si_3N_4 trapping layer to substitute poly silicon which were used in traditional floating gate memory device. Compared to the traditional floating gate memory device, SONOS flash memory device has a higher reliability, lower operation voltage and power consumption etc…

Reliability is one of the most important analysis for memory device. Endurance, retention, operation window, programming time … are included in reliable analysis. However, in our study we will focus on operation window.

We will use Silvaco TCAD to build a simple SONOS flash memory device. Changing the device's structure of tunneling oxide without disturbing other structures. We will simulate and analyze, when the device can operate with the best performance. Result of our simulate indicates that the device will have three regions for changing tunneling oxide thickness. Those regions will have different main influences. In the study 5.5nm tunneling oxide will have the most favorable operation window.

Furthermore, we used the result of the first study and changed the doping of the silicon in its bulk structure. Our studies found that when the device is in heavy doping ($n = 10^{20}cm^{-3}$), the substrate doping will change from $p = 5 \times 10^{16}\ to\ 1 \times 10^{17}cm^{-3}$. The result is similarly to the previous study that will have the favorable operation window at 5~6nm. To conclude, when the device is in lightly doping ($n = 10^{17}cm^{-3}$), the substrate doping will change from $p = 5 \times 10^{15}\ to\ 1 \times 10^{16}cm^{-3}$. Then, 4~5nm tunneling oxide will have more favorable operation window.

Therefore, when we combined two result of our study. The SONOS flash memory that we constructed in heavy doping ($n = 1 \times 10^{20}cm^{-3}, p = 1 \times 10^{17}cm^{-3}$), will have the most favorable operation window at tunneling oxide for 5nm. Then, in lightly doping (n =

$1 \times 10^{17}\text{cm}^{-3}, \text{p} = 1 \times 10^{16}\text{cm}^{-3}$), will have the most favorable operation window at tunneling oxide for 4nm.

INTRODUCTION

SONOS 元件，以其結構命名，是以矽-氧化矽-氮化矽-氧化矽-矽的堆疊結構組成。SONOS 快閃式記憶體元件與傳統浮動閘記憶體元件比較上，有著較簡易的結構、能在低電壓下操作、高度可靠性以及低功率等優勢。SONOS 元件利用閘極的高偏壓，使通道區產生載子穿隧的效應，電子穿過氧化層儲存在氮化矽的陷位中。當閘極施加高偏壓時，此時氮化矽層中的深層缺陷捕捉載子，電子數量增加，得到一個相對較高的臨界電壓(Threshold voltage, V_{th})，形成 "1" 的狀態，也可以稱作"被寫入(Programed/Charged)"。當閘極施加負偏壓時，在儲存層中的電子會穿隧回本體層，使得臨界電壓向左移，即為"0"的狀態，也可以稱作"被抹除(Erased)"。本專題中模擬主要採用熱載子效應(Hot carrier)與 F-N 穿隧效應(Fowler-Nordheim Tunneling)，分別用於寫入資料以及消除資料，藉由熱電子注入的方式來讓電荷儲存在氮化矽層的兩側達到儲存的二位元效果。

我們所設計的SONOS元件架構如FIG.1所示，本專題中嘗試利用模擬軟體來分析更改穿隧氧化層的厚度變化以及摻雜濃度的變化下操作區間的改變情形。此研究主要關注於操作區間的效果，因此在其他可靠度上不一定是最佳的情況，並且因為使採用模擬，在格點切割分析模擬上會有些誤差以及不準確，我們大都以整體趨勢為主要判斷依據。因此在兩項變化上能面對不同需求下，設計出較高操作區間的SONOS快閃式記憶體元件。

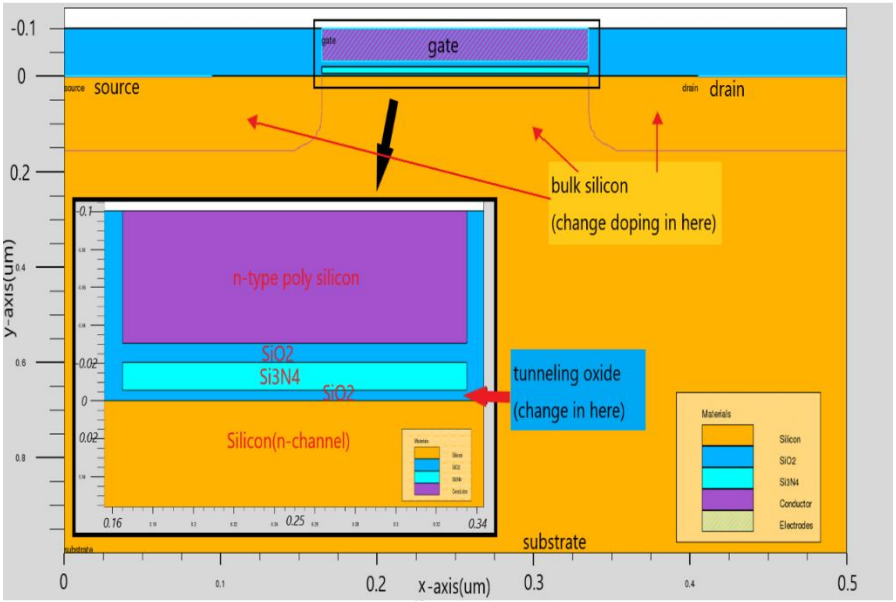

FIG. 1

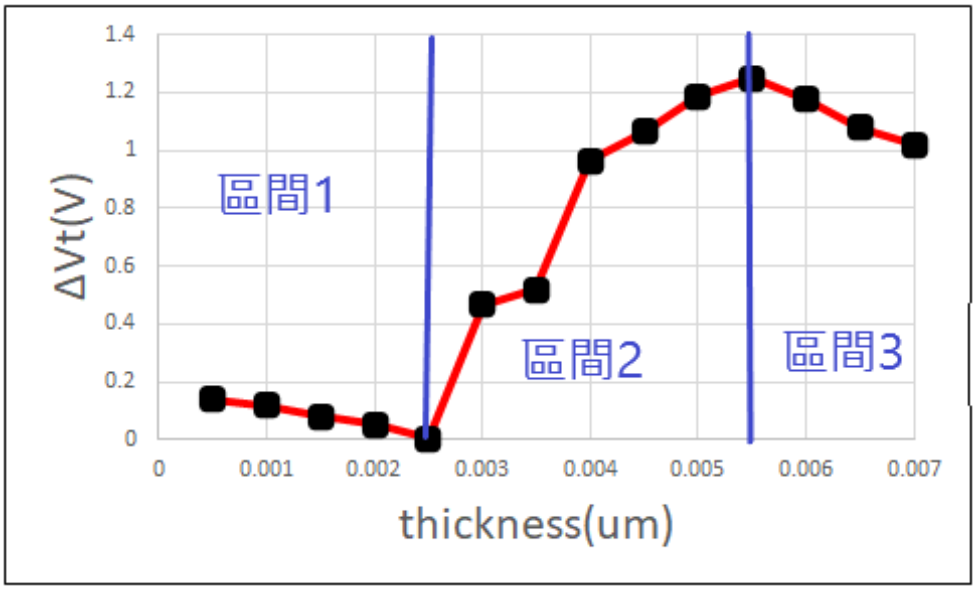
1.4
1.2
1
0.8
0.6
0.4
0.2
0
ΔVt(V)
區間1
區間2
區間3
0
0.001
0.002
0.003
0.004
0.005
0.006
0.007
thickness(um)

FIG.2

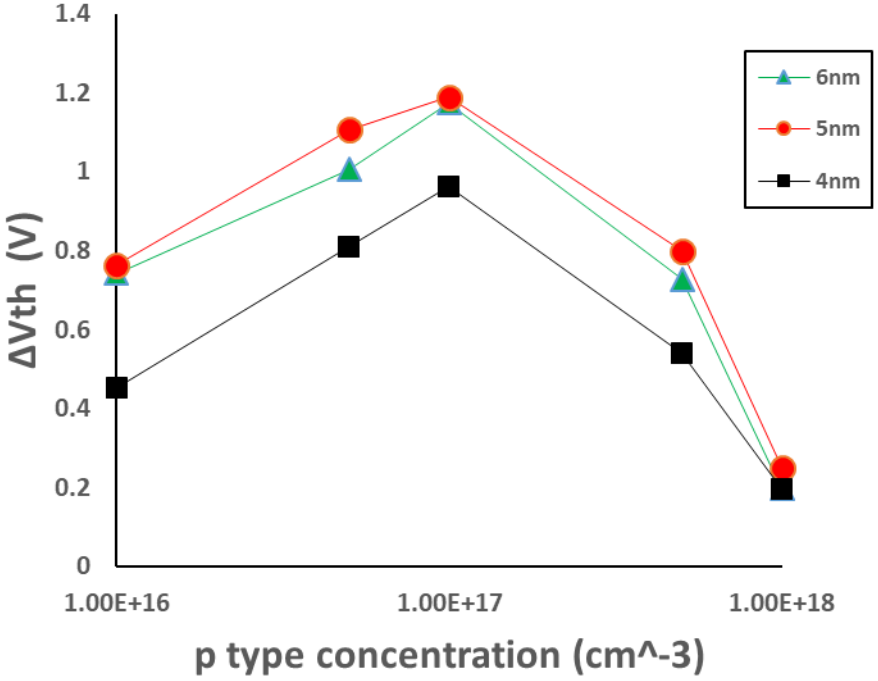
1.4
1.2
1
0.8
0.6
0.4
0.2
0
ΔVth (V)
6nm
5nm
4nm
1.00E+16
1.00E+17
1.00E+18
p type concentration (cm^-3)

FIG.3

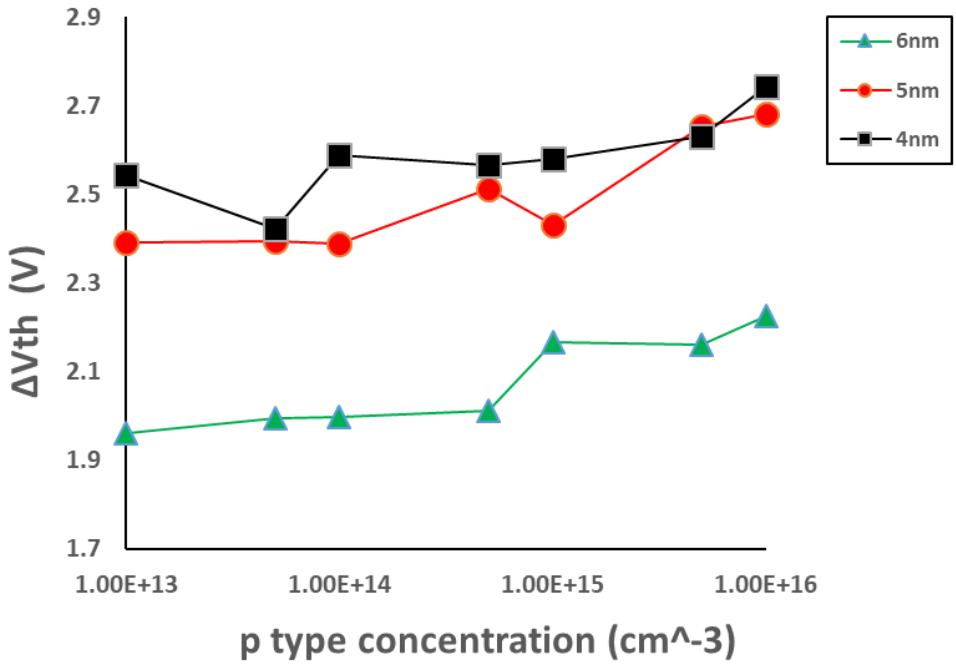

FIG.4

心得感想

經過一年的專題，我們對於元件的運作上有了更深入的了解。過程中面臨到了很多在修習相關課程不會遇到的問題，必須想辦法用實際理論或實驗數據來佐證我們提出的結論。整個過程中，我們深刻體會到做研究的不容易，雖然中途遭遇了不少挫折，在教授的耐心指導下，讓我們能更有效率的改善問題。