An 8-Bit 8-MS/s 1-V SAR ADC with Charge-Sharing Switching Method

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Abstract

As integrated circuit fabrication technology continues to scale down, low power and high efficient data converters can be implemented. In the case of low to medium resolution converters, most of the energy is consumed during the signal quantization process. The efficiency of this process is typically measured by the energy consumed per conversion step, known as the Walden figure of merit (FOM). In advanced CMOS processes, the FOM of successive-approximation-register (SAR) A/D converters can be lower than 3 fJ per conversion step. Historically, high-speed converters were favored, but they often came with high power consumption. However, with the growing demand for biomedical electronics and portable devices, there is increasing emphasis on designs that balance both performance and energy efficiency.

SAR ADCs (Successive Approximation Register Analog-to-Digital Converters) convert an analog input signal into digital code through a series of successive bit trials. In many reported designs, the DAC of a SAR ADC is capacitive and operates based on the charge-redistribution (CR) principle. Alternatively, a SAR ADC based on the charge-sharing (CS) principle presents an entirely passive operation after the pre-charge phase, obviating the reference buffer. Charge-redistribution SAR converters rely on an accurate reference voltage during these trials, typically provided by a large off-chip decoupling capacitor or a high-speed buffer. During a single SAR ADC conversion, the reference voltage must settle at least N times (where N is the resolution of the ADC), which means the settling time often consumes a significant portion of the total conversion time. When the sampling rate exceeds the MSPS (Million Samples Per Second) rate, the reference voltage settling becomes more demanding, often limiting the achievable linearity of the ADC.

To overcome this speed limitation, a passive-charge-sharing SAR ADC [1] pre-samples the reference voltage on-chip. It then uses the pre-sampled reference charge to carry out the bit trials. While this architecture may appear similar to the charge-redistribution design, it is fundamentally different. To differentiate, the traditional charge-redistribution SAR ADC is referred to as “active charge redistribution”, while the charge-sharing SAR is called the “passive-charge-sharing” SAR.

In the active charge redistribution system, a fixed voltage reference supplies any additional charge needed to rebalance the sampled signal. In contrast, the passive charge-sharing system uses a pre-sampled reference charge to rebalance the signal. The key difference is that the active system maintains a fixed voltage and supplies variable charge, while the passive system starts with a fixed charge and adjusts to a variable voltage. In summary, this represents a new type of SAR ADC. In this process, one charge sample is variable, while the other starts with a fixed charge and needs to adjust to a varying voltage.

Several techniques are used in this work to achieve a low-voltage and energy-efficient 8-bit CS-SAR ADC. The charge sharing DAC switching method introduced in this work can lower the power consumption of the capacitive DAC switching power without causing the linearity degradation typically seen in conventional charge re-distribution DACs.

1. Preface

This research presents a passive-charge-sharing successive approximation register (SAR) analog-to-digital converter (ADC) that achieves 8-bit linearity and 8MS/s operating rates with 1-V supply voltage in TSMC 180nm process, aims to mitigate the critical drawbacks of the architecture and allow the design of energy-efficient SAR ADCs for low-medium speed and low-voltage applications.

2. Operating Principle

The proposed CS-SAR ADC in this work includes sample and hold (S/H) circuitry, a digital-to-analog converter (DAC), a voltage comparator, and a digital SAR logic controller, the digital SAR logic controller contains an Asynchronous Control Logic and a DAC control. Figure 2.1 shows the block diagram of CS-SAR ADC.

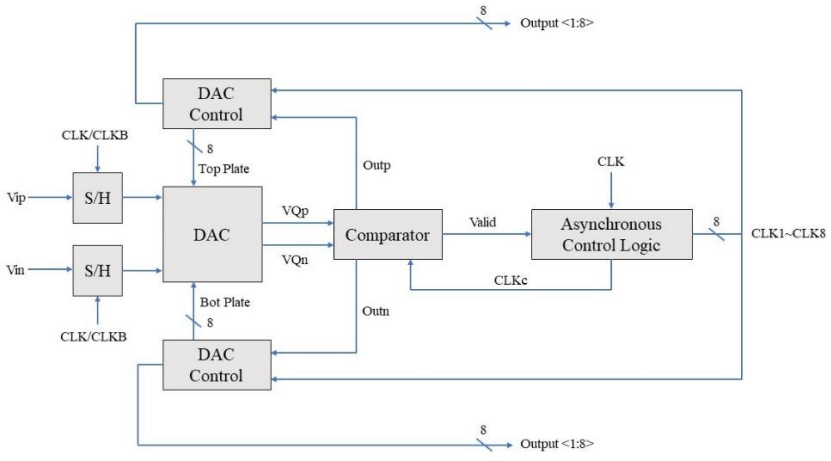

Figure 2.1 Block diagram of CS-SAR ADC

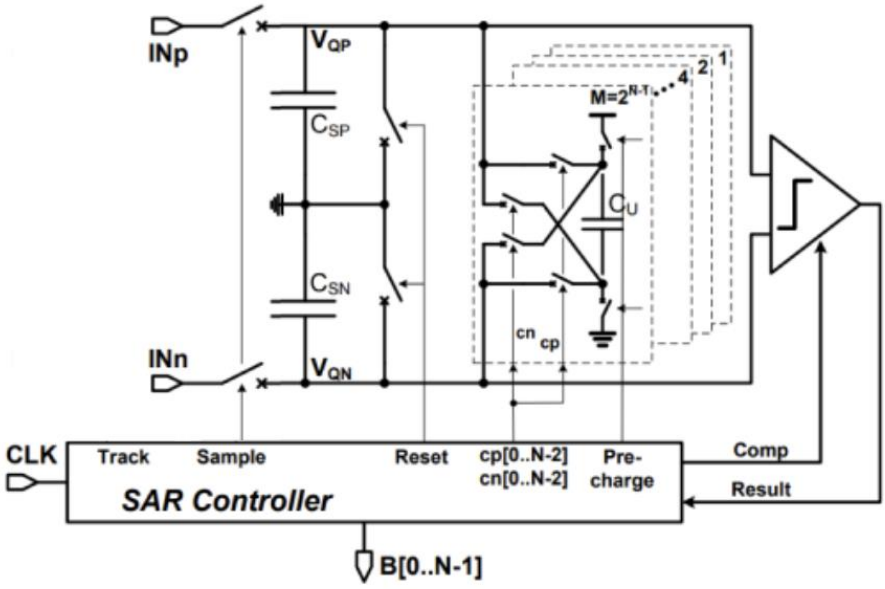

Figure 2.2 Charge sharing DAC switching schematic

The operation process of a charge sharing SAR ADC is as follows: sample and hold circuitry samples the differential input V_{ip} and V_{in} based on the clock signal. The two sampled data then preserve in the top plate and bottom plate of DAC respectively. After the comparator compares the voltages of the top and bottom plates, it outputs a signal named Valid. The Valid signal will enter the Asynchronous Control Logic and generates Clk_c signal and Clk_1~Clk_8 signals. The Clk_c signal will be fed back to the comparator to control when comparator start to work, while Clk_1~Clk_8 signals will be connected to the DAC control, and DAC control will generate outputs B1~B8, which will further control the switches on the weight capacitors inside the DAC (Figure 2.2). Output signal $B_1 \sim B_8$ will control the switches on the capacitor to determine whether to connect it is connected in parallel or anti-parallel to the top and bottom plates. Take first comparison for example, if VQP > VQN, the output signals B_1 and B_1_bar will control the switches on the capacitor to connect in is connected in anti-parallel. After this, the voltage VQP will become less than VQN. Repeating this process 8 times will bring the average voltage across the upper and lower boards closer to the input common-mode voltage. This process is known as binary search algorithm. In the end, we successfully convert an analog signal at a certain moment into an 8-bit digital signal.

The fully operation of differential CS-SAR ADC is depicted in Figure 2.3 and Figure 2.4. The voltage at the comparator inputs during a complete 8-bit conversion is for a 0.8V differential input with 0.5V common-mode and 1V reference voltage. In the first decision cycle, the inputs are sampled in the S/H, that is implemented explicitly in the CS scheme. Simultaneously, the capacitances in the array are pre-charged to $V_{PC} = V_{DD}$. In the following decision cycle, the comparator is activated, evaluating the voltage on the S/H to decide the MSB. According to the result, the largest capacitor on the array is connected in

parallel or anti-parallel to the S/H, adding or subtracting charge, respectively. This procedure is repeated for the other bits, as the differential voltage at the comparator inputs decreases towards zero and the comparison results are stored to form the digital output. The common-mode voltage at the comparator inputs is maintained constant in this scheme and equal to the input common-mode voltage. Figure 2.4 shows a deeper glimpse to CS switching scheme and conversion procedure, taking 2-bit for example briefly.

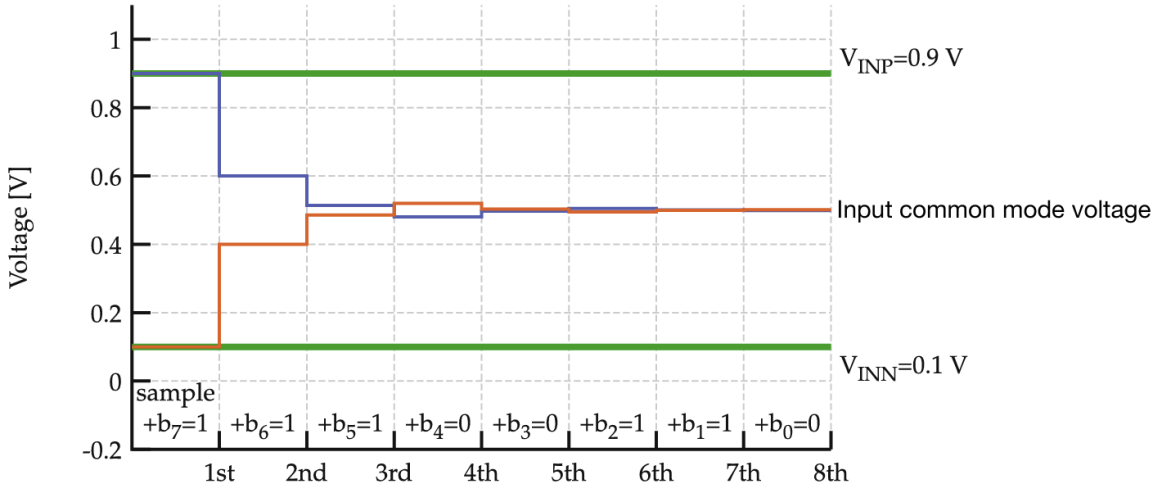

Figure 2.3 Comparison and bit decision cycle (Ideal Case)

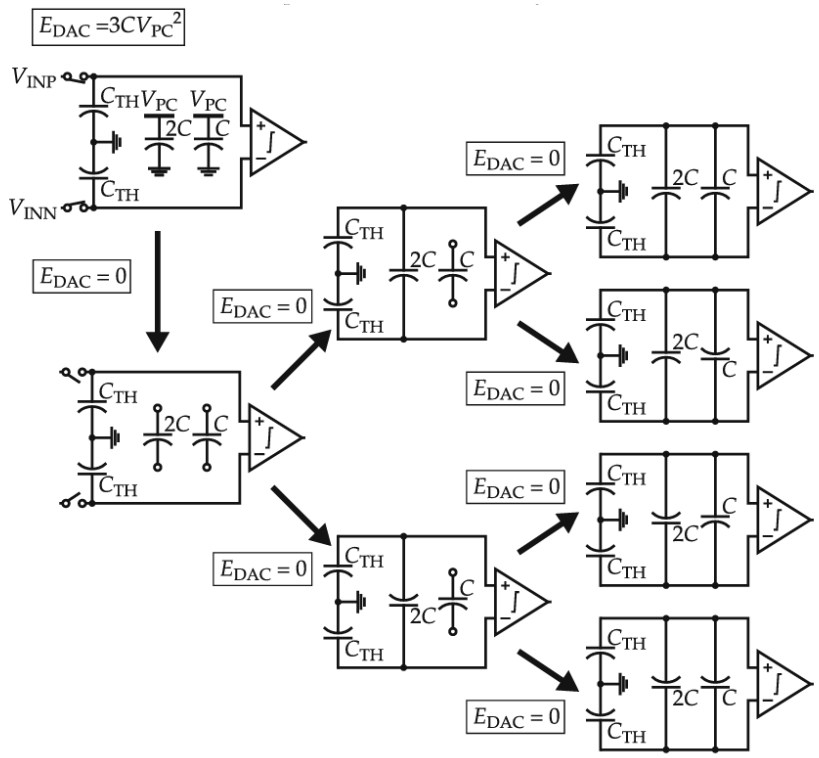

Figure 2.4 A deeper glimpse to CS switching scheme and conversion procedure

3. Simulation Result and Layout

3-1. Sample and Hold Circuit Simulation Result

The Sample & Hold operates with 8 MHz sampling frequency to sample a 3.96875 MHz sinewave differential input ($f_{Sample} * \frac{N_{FIN}}{N_{SAMPLE}} = 3.96875\ MHz$). The values in Table 1 and Table 2 represent the ENOB obtained from the sampling results for Pre-sim and Post-sim, respectively. Since our circuit is an 8-bit ADC, we aim for the Sample & Hold to achieve a resolution of at least 12 bits for high accuracy. As seen from Table 1 and Table 2, although the Post-sim ENOB is slightly lower than the Pre-sim ENOB, the ENOB across all corners still exceeds 12 bits.

ENOB	TT	FF	SS	FS	SF
Pre-sim	14.214	14.082	13.563	13.798	13.466
Post-sim	13.995	13.804	13.131	13.490	13.142

Table 3.1 Sample & Hold Pre-sim & Post-sim simulation result

3-2. Comparator Simulation Result

Table 3.2 shows the pre-sim and post-sim result of comparator. Take parasitic capacitance in layout in consideration, the comparing time increases by 80% in average. Furthermore, a supply voltage of 1 volt drastically slow down the comparison. However, before post-sim, we had accounted for extra time, so post-sim is still able to complete the 8-bit comparison within the conversion phase. On the other hand, the difference of power consumption between pre-sim and post-sim are not so much.

	Comparing Time		Power Consumption	
Corner	Pre-sim	Post-sim	Pre-sim	Post-sim
TT	0.58 ns	1.05 ns	14.4 μW	14.9 μW
FF	0.55 ns	0.98 ns	13.9 μW	14.3 μW
SS	1.59 ns	3.58 ns	17.3 μW	18.1 μW
FS	0.78 ns	1.35 ns	15.9 μW	16.2 μW
SF	1.37 ns	3.67 ns	17.0 μW	17.8 μW

Table 3.2 Comparator Pre-sim & Post-sim simulation result

3-3. CS-SAR ADC Simulation Result

Table 3.3 shows the ENOB simulation results for the CS-SAR ADC at 25°C, with a sampling rate of 8 MHz and an input signal frequency of 3.96875 MHz, for both pre-sim and post-sim across different corners. Since inevitably using large capacitance, the layout area is pretty large, resulting large parasitic capacitance that affect the performance.

Corner / ENOB	Pre-sim	Post-sim
TT	8.201	8.193
FF	8.154	8.052
SS	8.146	8.036
FS	8.158	8.077
SF	8.066	8.041

Table 3.3 CS-SAR ADC Pre-sim & Post-sim result

3-4. Power Dissipation

Table 3.4 shows the average power dissipation lasting for a period of overall CS-SAR ADC for both pre-sim and post-sim. The sources of power include VDD S/H (voltage source for sample and hold circuit), VDD_ref (reference voltage for DAC), VDDA (voltage source for analog circuit), and VDDD (voltage source for digital circuit), which are directly summed in the table. We can observed that the average power dissipation between pre-sim and post-sim increased by 110% after taking all parasitic capacitance into consideration, as well as the effect raised by routing.

Corner / Avg. Power (μW)	Pre-sim	Post-sim
TT	120.46	263.88
FF	114.72	251.78
SS	115.12	254.19
FS	114.56	260.60
SF	123.55	268.55

Table 3.4 Average power dissipation Pre-sim & Post-sim result

3-5. Layout

Chip Size: 1198.45um x 884.35um
Transistor / Gate Count: 3001 transistors
Power Dissipation: 263.88μW (Full chip @TT corner)

Max. Operating Frequency: 8MHz

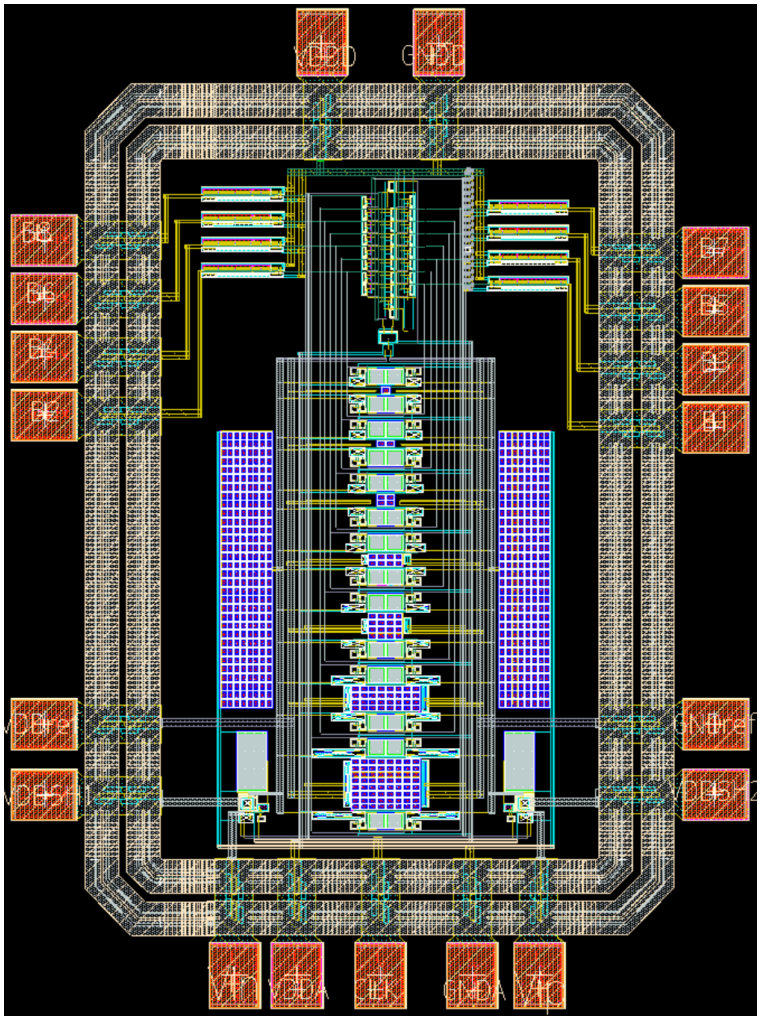

Figure 3.1 Layout

Specification	This work
Technology (nm)	180
Supply Voltage (V)	1
Sampling Rate (MS/s)	8
Resolution (bits)	8
ENOB (bits)	8.193
ERBW (MHz)	4
Power (μW)	263.88
FOM (fJ/Conv.step)	112.7
Area (mm^2)	1.059

Table 3.5 CS-SAR ADC Performance Summary

Reference	[1]	[7]	[8]	[9]	[10]	This work
Technology (nm)	90	40	130	180	130	180
Supply Voltage (V)	1	1.1	0.6	0.6~1	0.6	1
Operating mode	CS	CS	CS	CS	CS	CS
Sampling Rate (MS/s)	20	80	1	0.0022~1.5	0.2	8
Resolution (bits)	9	10	9	9	8	8
Power (μW)	290	5450	2.78	0.77~20.5	3.44	263.88
FOM (fJ/Conv.step)	65	85	7.8	32~79	12.5	112.7

Table 3.6 Performance Summary and Comparison

4. Conclusion

In this work, a passive charge-sharing successive approximation register (SAR) analog-to-digital converter (ADC) has been designed and implemented to achieve 8-bit linearity and 8 MS/s operating rates with a 1-V supply voltage, fabricated using TSMC 180nm process. The design successfully leverages the simplicity and power efficiency of the passive charge-sharing technique while maintaining high performance in terms of resolution and conversion speed.

Key results demonstrate that the proposed ADC meets the required specifications, including linearity, resolution, and sampling rate, even with the constrained 1-V supply. The use of passive components for charge sharing helps minimize power consumption, making it suitable for low-power applications. Furthermore, the integration of a SAR logic controller ensures high-speed operation while keeping the overall circuit area compact.

This implementation proves that it is possible to achieve an efficient, low-voltage SAR ADC with good linearity and high sampling rate in a standard CMOS process, which can be applied to various applications requiring low-power, high-speed, and compact ADC solutions. Future work could focus on further improving the linearity and speed of the design, possibly through circuit optimization or advanced techniques like calibration or dynamic element matching.

5. References

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6. Experience and Thoughts

在完成這個專題後，我發現之前 AIC、VLSI 兩門課的作業和 final project 都非常的基礎，雖然有跑 pre-sim、post-sim、完成 layout 等等，但對於一個要下線的電路而言，在設計時還必須考慮許多在課堂被視為理想或不考慮的效應。例如 noise、 mis-match、offset、寄生電容，尤其是在畫 layout 時要考慮對稱性或如何走線，要構想很久。但我從中學習到很多 layout 的技巧並實作，例如用 guard ring 來保護對訊號敏感的類比電、考慮真實製程的效應而將各個 MOSFET 加上 dummy structure、MOM 電容的畫法、IO PAD 的考量與規劃等等，這些都是我在做專題之前都不知道的事。這九個月來，我覺得自己在電路設計方面有很大的進步，獲得了寶貴的知識與經驗，這些知識與經驗是無法透過修課獲得的。專題與一

般課程不同於通常沒有標準答案，不像 AIC 電路架構都選好了，只需要達到 spec 就好，必須從論文與實際模擬中去學習與觀察，並找到最佳解。

非常感謝黃柏鈞老師讓我有這個機會更深一層的接觸類比電路的世界，每週的 meeting 後總能收穫到很多，並加以改進。雖然一個人一組真的蠻硬的，常常都做到天亮，但回過頭看自己一組才能學的最紮實，感謝教授安排這麼充實的專題課程，在 PCLAB 裡學到很多東西，最後順利完成。