國立清華大學 電機工程學系
實作專題研究成果摘要

Department of Electrical Engineering, National Tsing Hua University
Special Topic on Implementation Research Summary

A K-Band GaN MMIC Voltage Controlled Oscillator with High Output Power and Low Phase Noise
K頻帶低相位雜訊及高輸出功率之氮化鎵微波單片集成壓控振盪器電路

專題領域(Major Category)：電子領域 (Electronics)
組　　別 (Team) ：B332
指導教授(Advisor)：徐碩鴻 Shawn S.H. Hsu
組員姓名(Member)：魏鳳廷 Feng-Ting Wei
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Abstract

This is a novel design for a monolithic microwave integrated circuit (MMIC) oscillator, characterized by low phase noise and high output power, specifically tailored for radar and satellite applications. This oscillator utilizes the WIN 0.25um RF High Power GaN-on-SiC HEMT Technology, enabling the creation of a compact microwave oscillator, and the design, optimization, and analysis of the oscillator are conducted by advanced design system (ADS) simulator. The resulting voltage controlled oscillator, measuring only 1mm^2 chip area, generates the frequency at K-band, within 21 GHz to 21.2 GHz and 1% of tuning range. The primary objective is to achieve high output power and low phase noise while adhering to specified criteria. The optimized microwave oscillator demonstrates promising outcomes, with the post-layout simulation of output powers of 16.8 dBm at 21 GHz and produces sinusoidal signals with amplitudes of 2.3 V. In addition, this design has a relatively low 0.61W power consumption compared with other works at similar output powers. The phase noise of the oscillator at 21GHz , utilizing the LC resonator, registers at -125.8 dBc/Hz at 1MHz offset and -149.7 dBc/Hz at a 10 MHz offset.

摘要

這是一種用於單片微波集成電路（MMIC）振盪器的設計，具有低相位噪聲和高輸出功率的特點，專門為雷達和衛星應用而設。該振盪器利用WIN 0.25um RF高功率GaN-on-SiC HEMT技術，實現了緊湊的微波振盪器的創建，並透過Advanced Design System（ADS）模擬進行了振盪器的設計、優化和分析。結果得到的電壓控制振盪器，僅占用1mm^{2}芯片面積，並在K頻段生成頻率，在21 GHz至21.2 GHz之間，且調頻範圍為1%。主要目標是在遵循指定標準的同時實現高輸出功率和低相位噪聲。經過優化的微波振盪器展示了令人期待的結果，21 GHz的後佈局模擬輸出功率為16.8 dBm，並生成振幅為2.3 V的正弦信號。此外，與相似輸出功率的其他作品相比，該設計的功耗相對較低，為0.61瓦。振盪器在21 GHz時使用LC諧振器，1 MHz偏移時的相位噪聲為-125.8 dBc/Hz，10 MHz偏移時為-149.7 dBc/Hz。

Background and Motivation

A monolithic microwave integrated circuit (MMIC) is a compact integrated circuit device with dimensions typically ranging from around 1 mm² to 10 mm², allowing for large-scale production. This work specifically employs GaN HEMT as the active device in this MMIC, due to its capability for high-speed and high-power operation in comparison with CMOS. Leveraging these advantages, it is more advantages to design an oscillator with a greater output swing, which is beneficial for enhancing two crucial performance factors: reducing phase noise and increasing output power. Furthermore, K-band frequency is best-suited for short-range communication, especially in speed and safety radars. For such applications, K-band monolithic microwave integrated circuit (MMIC) technology is an emerging trend that helps realize K-band oscillators on a small die with reduced costs, ease of mass production, and high reliability.

Many electronic applications require the frequency of a signal to vary constantly. Phase-Locked Loop (PLL) is one of the example: to match the frequency/phase of the input reference signal using the feedback loop to control system to alter the frequency and/or phase of the oscillator. This is where the function of a Voltage-Controlled Oscillator (VCO) comes into play. The design purpose of such components is that the generated output signal frequency varies within a reasonable frequency range with the voltage amplitude of the input signal.

Method

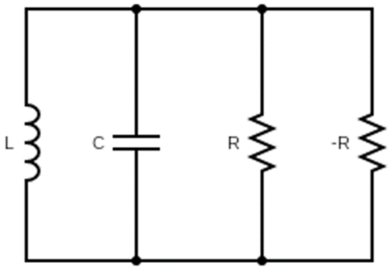

Fig. 2.2.1 Basic Oscillator Structure

The basic oscillator architecture consists of two main components (Fig. 2.2.1): (1) LC tank and (2) negative impedance or positive feedback system. Because LC components inherently have losses and cannot sustain oscillation, it is necessary to provide negative impedance through the characteristics of active components to counteract the losses of LC elements. The oscillator design in this work employs the traditional Cross-Coupled Pair (Fig. 2.2.2) to provide negative impedance for the continuation of oscillation.

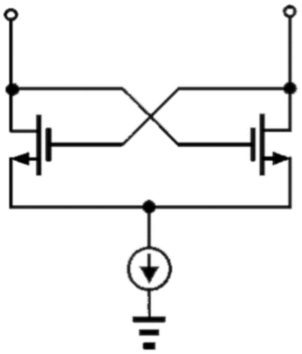

Fig. 2.2.2 Cross-Coupled Pair

In terms of oscillator performance, phase noise plays a particularly crucial role. Many studies have explored methods to reduce phase noise, such as increasing the swing of the oscillator or using inductors and capacitors with high Q values to reduce the decay and noise of the LC tank. In addition to selecting V_{dd}, I_{bias}, and inductance to maximize the oscillation swing as much as possible, this design also incorporates a matching network at the output to further maximize the oscillation swing.

This design can be divided into three stages, namely (1) LC tank design, selection of inductance, and HEMT design; (2) Output Matching design; and (3) Bypass design.

Result

A. Post-layout Simulation of Output Signal Waveform and Start-up Time at Temp=25 °C

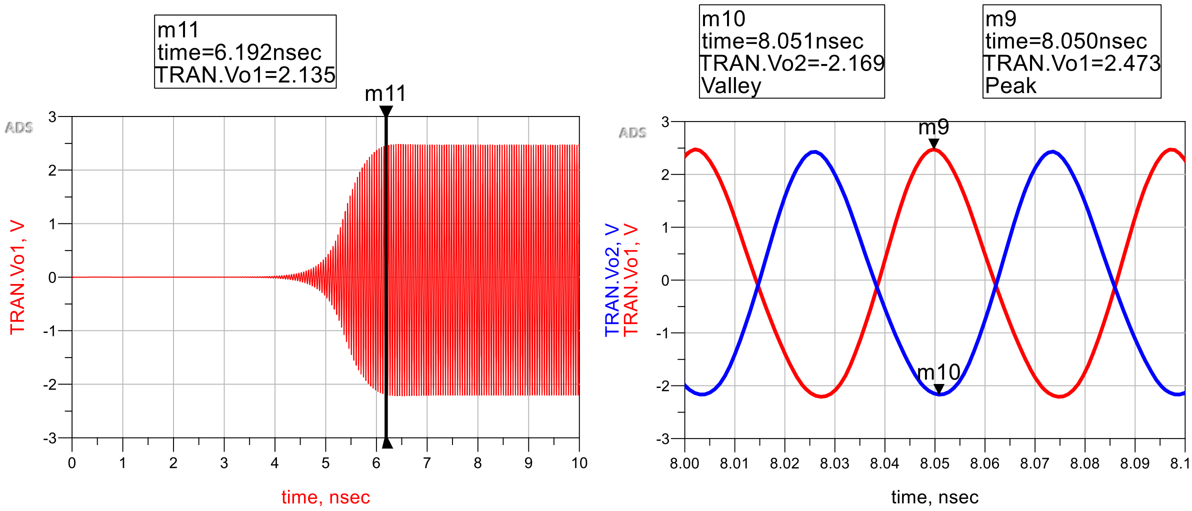

Fig. 4.1.1 Transient analysis of output signal

- Oscillation Start-up time = 6.2 ns
- $V_{\text{peak-to-peak}} = 4.65\text{V}$

B. Post-layout simulation of Harmonic Balance Analysis at Temp=25°C

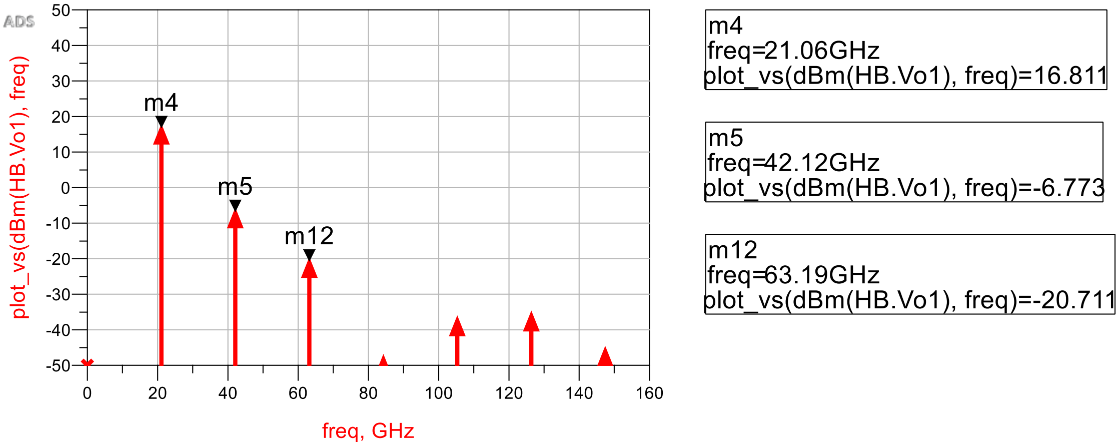

Fig. 4.1.2 Harmonic balance analysis of output power

- At fundamental frequency: 16.8 dBm
- 2nd harmonic: -6.8 dBm
- 3rd harmonic: -20.4 dBm

C. Post-layout simulation of Phase Noise at Temp=25^{o}C

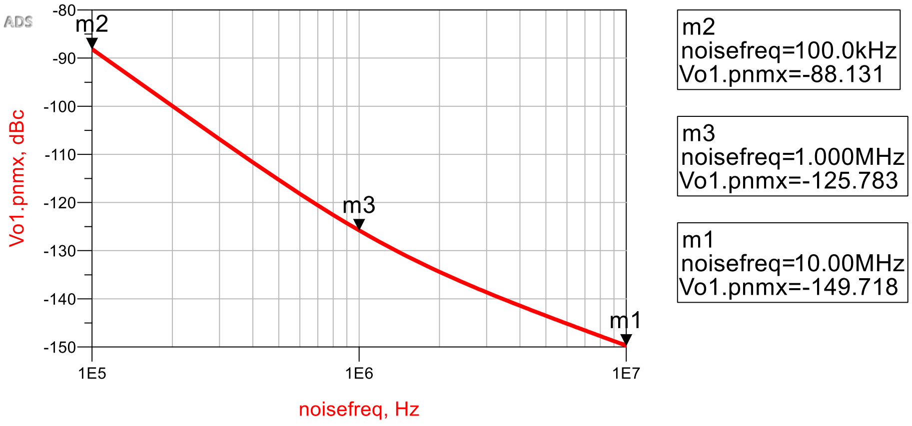

Fig. 4.1.3 Phase noise simulation at 21GHz at 100kHz, 1MHz, and 10MHz offset

- At 100kHz offset: -88.1 dBc/Hz
- At 1MHz offset: -125.8 dBc/Hz
- At 10MHz offset: -149.7 dBc/Hz

D. Post-layout Simulation of Harmonic Balance Analysis Sweeping Vdd @ Vg=-1.4V at Temp=25^{o}C

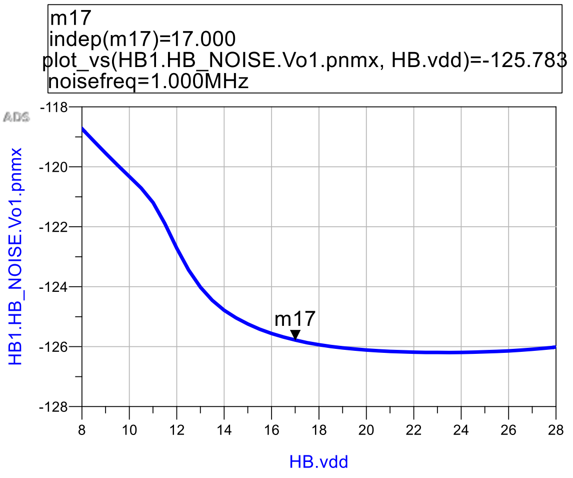

Fig. 4.1.4 phase noise vs. vdd sweep plot

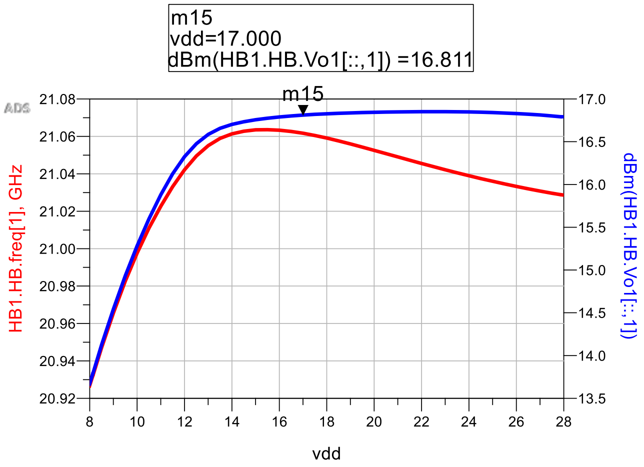

Fig. 4.1.5 frequency and output power vs. vdd sweep plot

- These figures show that VDD at 17V has the best performance

E. Post-layout Simulation of Harmonic Balance Analysis Sweeping Vg @ Vdd=17V at Temp=25^{o}C

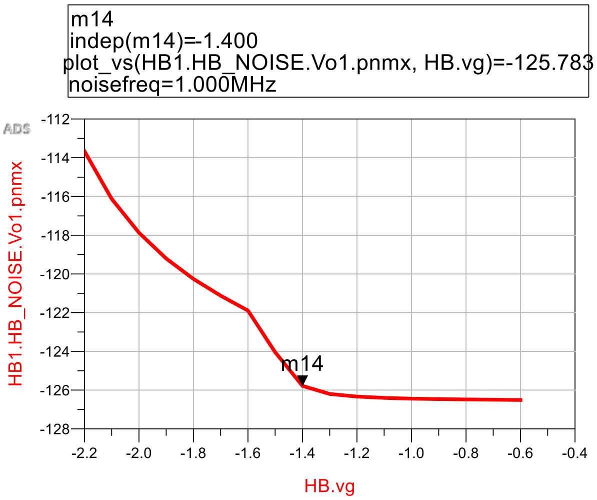

Fig. 4.1.6 phase noise vs. vg sweep plot

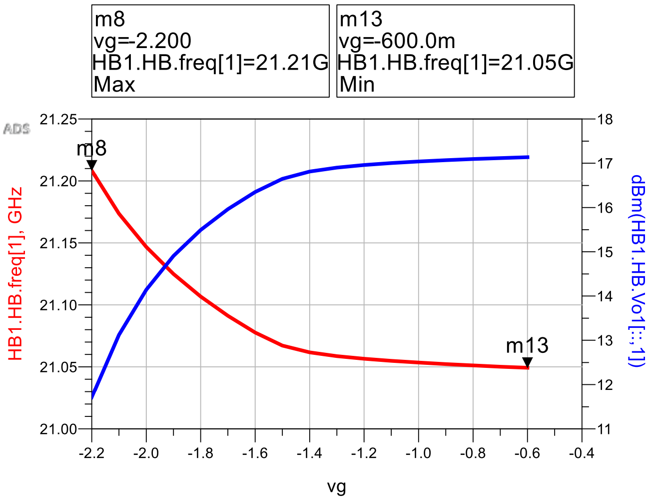

Fig. 4.1.7 frequency and output power vs. vg sweep plot

- These figures show that at Vg at -1.4V has the best performance

Parameter	**[4]**	**[3]**	**[2]**	**This work**	**SPEC**
Process	GaN25	GaN25	GaN25	GaN25	GaN25
Power Suppy (V)	19	----	----	17	---
DC Power [mW]	2204	1456	747	608.6	---
Output Power [dBm]	27.9	21	16	16.8	---
DC to RF Efficiency	28%	8.6%	5.3%	4.5%	---
Tuning Range	1.1%	----	2.1%	1%	---
Size [mm^2]	3	0.66	0.71	1	=1mm^2
Phase Noise@1MHz [dBc/Hz]	-121.6	-135	-109.4	-125.7	<-110
Frequency [GHz]	9.35~9.46	7.9	23.9~24.4	20.9~21.1	>20
FoM [dBc/Hz]	167.6	-181.3	-176.8	-184.3	<-180

Table 4.3.1 Performance comparison with reference paper

Conclusion

This research introduces a K-band MMIC cross-coupled oscillator leveraging 0.25-µm GaN HEMT technology. A meticulous analysis and design of the coupling capacitors within the core circuit were conducted to achieve exceptionally low phase noise, incorporating a specifically designed spiral inductor to attain the desired frequency. The size and bias of the HEMT were carefully selected to optimize both high output power and relatively low power consumption.

In lieu of employing a buffer stage, an output matching network was implemented to effectively match the fundamental signal to a 50Ω load while simultaneously filtering out undesired harmonic signals. The exhaustive efforts invested in this work resulted in an outstanding figure of merit of -184.3 dBc/Hz. As of now, the chip is currently under fabrication, with the anticipated chip completion date set for March 2024.

This study has successfully achieved a combination of low phase noise and high output power, making it highly promising for applications in radar or short-range communications. This underscores the considerable potential of GaN technology in millimeter-wave applications, showcasing its suitability even for outer space satellite communications.