國立清華大學 電機工程學系
實作專題研究成果摘要

Minimizing Timing Jitter in Single-Photon Avalanche Diodes Through Advanced Active Quenching Techniques

透過先進主動式淬熄技術降低單光子雪崩二極體的時間抖動

專題領域：光電領域

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Abstract

Single-photon detection refers to methods that, under extremely low photon flux, convert single-photon events into measurable electrical/digital signals. Its applications span distance measurement and 3D imaging, quantum communications, and astronomical observations. The goal of this technology is, within the target spectral band and application context, to acquire—with near-zero distortion—the time of arrival (TOA) and pixel/position information of each photon, while, under low-cost and low-power conditions, increasing detection efficiency (PDE) and maximum count rate and reducing dark count rate (DCR) and timing jitter.

Regarding detector choice, superconducting nanowire single-photon detectors (SNSPDs) currently offer the best system detection efficiency and ultra-low dark counts; however, they require cryogenic operation and complex systems and thus remain far from large-scale adoption. In the mass market, single-photon avalanche diodes (SPADs) dominate because they operate at room temperature, are compatible with CMOS integration, exhibit low timing jitter, and are readily arrayed. Silicon-based SPADs perform particularly well in the visible band, and recent back-side illumination (BSI) and 3D stacking have improved fill factor and system integration.

Given the operating principle of SPADs, an external quenching circuit is required to enable stable single-photon counting. Passive quenching (PQC) achieves automatic reset via a series resistor, but the recovery time is relatively long, limiting the maximum count rate and effective detection rate. In most cases, active quenching (AQC) is adopted to shorten the recovery time and reduce afterpulsing. In this project, we implemented and validated the AQC architecture proposed in [1] and completed the relevant simulations. In our design, we modified the circuit architecture to optimize the recovery time and perform measurements using a printed circuit board (PCB) to verify the feasibility of the proposed external AQC.

摘要

單光子偵測指在極低光子通量下，將單一光子事件轉換為可量測的電／數位訊號的方法。其應用涵蓋距離量測與 3D 成像、量子通訊以及天文觀測。此技術的最終目標，是在目標波段與應用情境中，以近乎零失真地取得每一顆光子的到達時間（TOA）與像素／位置資訊，同時在低成本、低功耗條件下提升偵測效率（PDE）與最大計數率、降低暗計數率（DCR）與時間抖動。

在偵測器選擇上，超導奈米線單光子偵測器（SNSPD）提供目前最佳的系統偵測效率與極低暗計數，惟需低溫且系統複雜，距離大規模普及仍遠。大眾市場則以單光子雪崩二極體（SPAD）為主，因其可在室溫運作、相容 CMOS 整合、時間抖動低且易於形成陣列，矽基 SPAD 於可見光波段表現尤佳，且近年背照式（BSI）與 3D 堆疊提升了填充率與系統整合度。

考量 SPAD 的工作原理，需搭配外部淬熄電路（quenching circuit）方能穩定地進行單光子計數。被動式淬熄（PQC）以串聯電阻達成自動復位，但恢復時間較長，限制最大計數率與有效偵測率。多數情況採用主動式淬熄（AQC）以縮短恢復時間並降低後脈衝（afterpulsing）。在本專題中，我們實作並驗證文獻 [1] 所提出的 AQC 架構，並完成相關模擬。在我們的設計中，調整了電路架構，優化其中的恢復時間，並利用印刷電路板進行相關量測，驗證所提外部 AQC 的可行性。

Contents

1. Background

With the rapid growth of 3D imaging, quantum communication, and high-speed photon counting, the performance of single-photon detectors has become a system bottleneck. While SNSPDs offer near-ideal detection capability, their cryogenic operation limits practicality. SPADs, in contrast, support room-temperature CMOS integration, but require an external quenching circuit that strongly affects key metrics such as recovery time, maximum count rate, afterpulsing, and timing jitter. Passive quenching circuits are simple but slow, whereas active quenching circuits (AQC) reduce recovery time and afterpulsing, yet still face challenges in avalanche detection latency, hold-off control, and parasitic effects.

This work proposes an improved AQC architecture featuring a low-latency avalanche detector and a fast recovery path that alleviates RC-related limitations. Circuit-level simulations are performed to analyze recovery time, count-rate capability, and afterpulsing across different excess-bias conditions, followed by PCB implementation for experimental validation. Results show that the proposed AQC effectively shortens recovery time and enhances detection performance without increasing power consumption or circuit complexity, demonstrating its practicality for next-generation single-photon detection systems.

2. Purpose

The purpose of this study is to design, optimize, and experimentally validate an improved active quenching circuit (AQC) for single-photon avalanche diodes (SPADs). This work aims to overcome key limitations of conventional quenching circuits—specifically long recovery time, high afterpulsing probability, and limited count-rate performance—while maintaining low power consumption and compatibility with practical room-temperature operation. By developing a low-latency avalanche detection path and a fast, controlled recovery mechanism, the proposed AQC seeks to provide a more efficient, stable, and integrable solution for high-performance single-photon detection systems.

3. Research Methodology

3.1 Research Framework

(1) Design the architecture of active quenching circuits

(2) Simulate it on HSPICE

(3) Confirm the corresponding block and find suitable component

(4) Draw PCB layout by these components

(5) Measure the PCB and analysis the result

3.2 Design of the Active Quenching Circuit (AQC)

The active quenching circuit (AQC) architecture adopted in this work is shown in Fig. 1, with a single-photon avalanche diode (SPAD) connected at the lower-right node. The overall circuit can be divided into two major functional blocks: avalanche detection and recovery, and output signal buffering. For avalanche detection, the circuit employs a two-stage inverter acting as a comparator. When the SPAD node voltage drops due to an avalanche, the comparator responds rapidly, enabling low-latency and low-noise detection of the avalanche event and ensuring timely control actions. Meanwhile, the PMOS transistor located below the V_{buffer} node determines when the SPAD re-enters its operating state. This design minimizes the dead time as much as possible to improve the photon detection efficiency (PDE).

The biasing and load path—provided by V_{bias} and the PMOS transistor at the upper-right—keeps the SPAD operating in Geiger mode and supports fast recovery in coordination with the detection circuitry. Finally, the output buffer converts the internally detected avalanche event into a stable external signal V_o, while preventing excessive loading from disturbing the SPAD node. By combining low-latency avalanche detection with a fast recovery mechanism, the proposed architecture effectively shortens the recovery time and delivers a clean output signal, forming the basis for subsequent simulation and PCB-level validation.

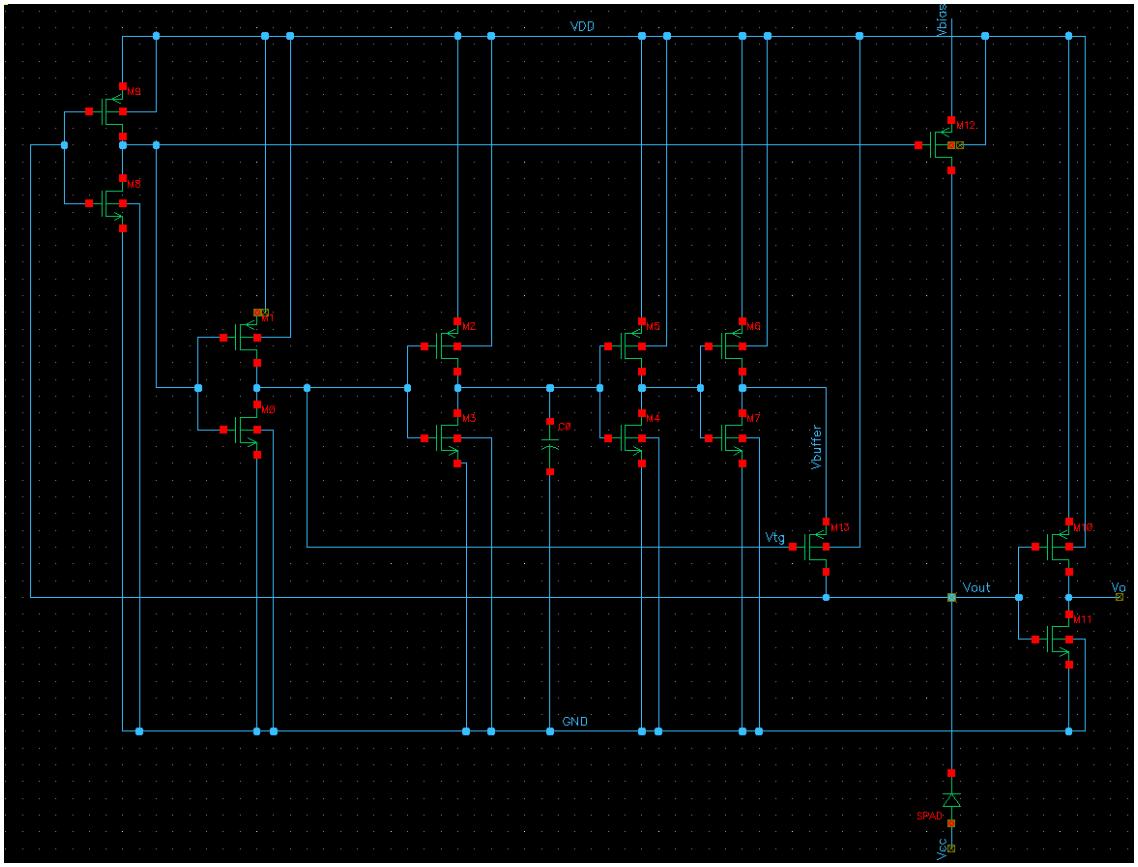

Fig. 1 AQC Architecture Proposed in This Work

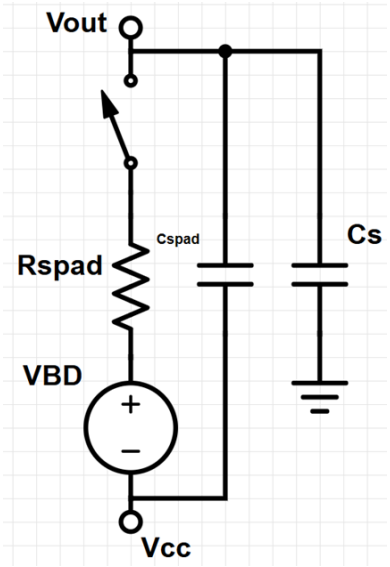

Fig. 2 SPAD Equivalent RC Model

3.3 Simulation Setup

In this work, HSPICE with the TSMC 180 nm process is used as the primary simulation platform to analyze the time-domain behavior and operational characteristics

of the proposed active quenching circuit (AQC). The SPAD is represented using a simplified equivalent model, as shown in Fig. 2, to emulate the avalanche current pulse triggered by a single-photon event. The SPAD breakdown voltage V_{BD} is obtained from measurement. For the SPAD used in this study, the breakdown voltage is 50 V, with $R_{spad} = 1000\Omega$, $C_{spad} = 10pF$, $C_S = 5pF$.

The simulation conditions are configured with the source voltage of most PMOS transistors set to $V_{DD} = 1.2V$, while GND serves as the source reference for the NMOS devices. The voltages V_{bias} and V_{cc} define the two terminals that control SPAD breakdown and must be maintained within specific ranges to ensure proper system operation. The temperature is set to 25 °C under the TT process corner. In this configuration, V_{bias} and V_{cc} are set to 0.7 V and –16 V, respectively. The SPAD is modeled to undergo breakdown at 1 ns and to cease the avalanche at 2 ns.

Based on the simulation conditions described in the previous section, the time-domain voltage waveforms at each node can be obtained. As shown in Fig. 3, V_{out} initially remains at a high level. Now of breakdown at 1 ns, it begins to drop, eventually falling below V_{buffer}. Once V_{buffer} transitions to a high level, the avalanche current is terminated. After the avalanche is quenched, the recovery process begins. The PMOS transistor below the V_{buffer} node turns on, causing V_{out}—which had been decreasing—to gradually rise back to its original state. The output signal V_o exhibits an opposite transition corresponding to the change in V_{out}. When V_{tg} returns to a high level, the PMOS turns off, and the entire system fully returns to its initial operating condition.

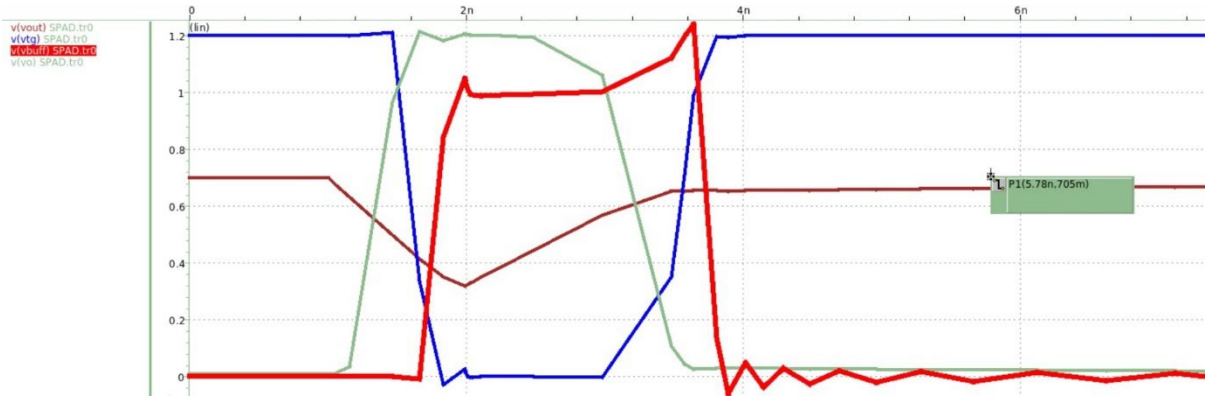

Fig. 3 Simulation Results of the AQC

3.4 PCB Implementation and Experimental Measurements

After completing the simulations, suitable electronic components were selected to implement the proposed AQC architecture. As the circuit consists of six inverters and two PMOS transistors, we sourced the components from the SnapEDA database. Specifically, the MC74AC14 Hex Inverter Schmitt Trigger was selected, along with the BSS83PH6327XTSA1 p-channel power MOSFET. These two IC components collectively fulfill the functional requirements of our circuit implementation.

Next, the three IC components were interconnected to realize the design shown in Fig. 1. The routing layout is illustrated in Fig. 4. The printed circuit board (PCB) was then implemented using Altium Designer, where the routing diagrams were translated into the final PCB layout. created under the design-rule constraints (DRC) required for TSRI PCB fabrication. The input and output nodes are interfaced using SMA connectors, which improve signal integrity and facilitates subsequent measurements.

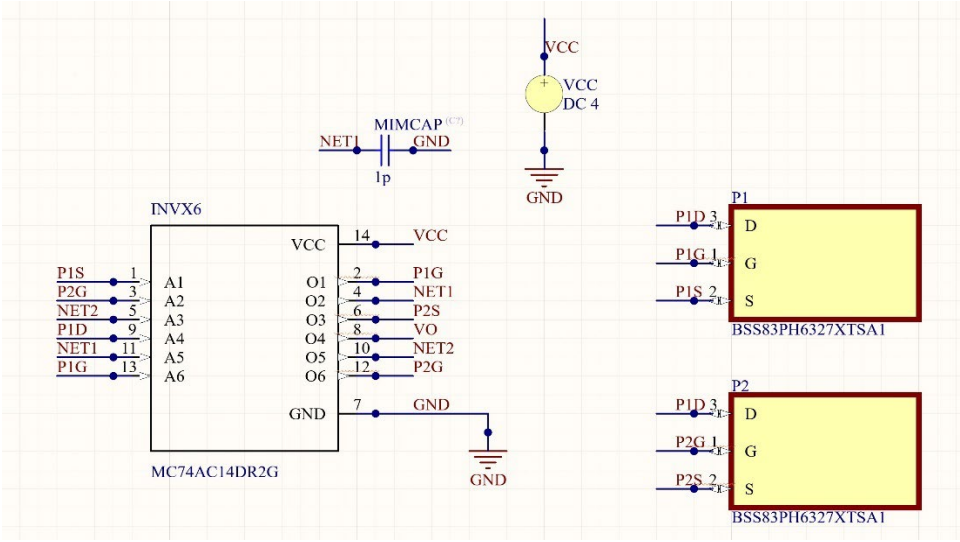

Fig. 4 External Layout of the IC Assembly

4. Results

4.1 Tuning some parameters

4.1.1 Tuning the MIM Capacitor:

The MIM capacitor was originally included to model the junction capacitance

corresponding to the 180 nm simulation process. However, after the PCB implementation, additional parasitic capacitances arise due to routing and interconnecting effects. Therefore, we varied the MIM capacitance value to evaluate how much these internal parasitic could influence the actual measurement results. From the figure below, it can be observed that the hold-off time increases linearly with the MIM capacitance. This trend explains why the measured delay on the PCB is larger than expected.

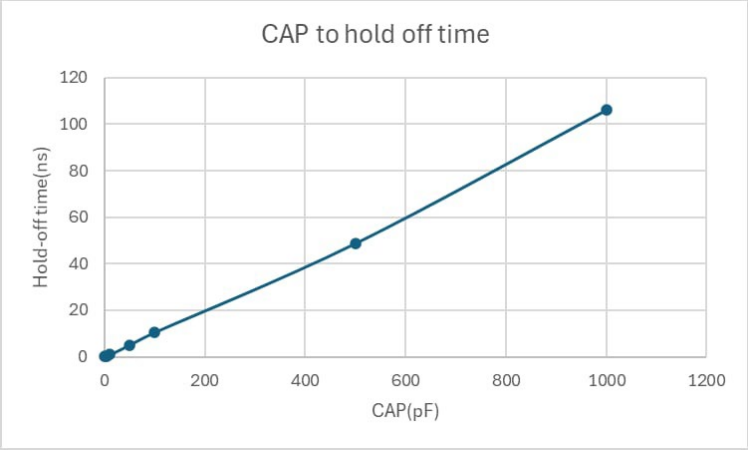

Fig. 5 Effect of MIM Capacitor on Hold-Off TimeV_{out}

4.1.2 Tuning the PMOS Width of M13:

Considering that the size of transistor M13 determines its voltage sensitivity and switching speed, increasing its width is expected to reduce the recovery time. A larger M13 allows V_{out} to return from a lower potential to a high level more quickly, thereby reducing the overall dead time.

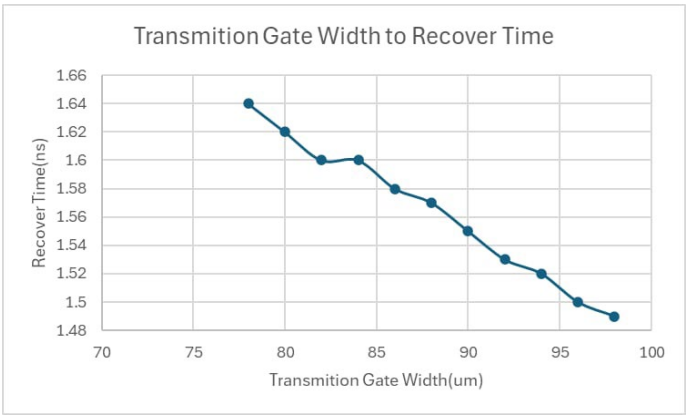

Fig. 6 Effect of PMOS M13 on Recovery Time

4.1.3 Tuning the PMOS Length of M12:

To ensure that the PMOS devices—other than the largest hex inverter—possess

sufficient sensitivity for proper current control, we analyzed the trend by modifying the PMOS responsible for detecting the avalanche current. When the PMOS channel length is increased from the original 180 nm to 2000 nm (brown to blue), the output V_o rises more rapidly. As a result, we can improve the rise time of V_o.

The purpose of adjusting this parameter is to reduce jitters, which can be understood as the timing error between when an event is expected to occur and when it occurs, the smaller this error, the better. In our simulation, V_{ctrl} represents the breakdown signal, while the other two waveforms correspond to different PMOS channel lengths as described above. From these results, we can conclude that increasing the PMOS channel length leads to a higher $R_{ds(on)}$, making the AQC more sensitive to the SPAD current. As a result, a smaller current is sufficient to trigger the quenching action, which shortens the rise time and consequently reduces jitter. This improvement enhances the timing resolution and yields more accurate event detection.

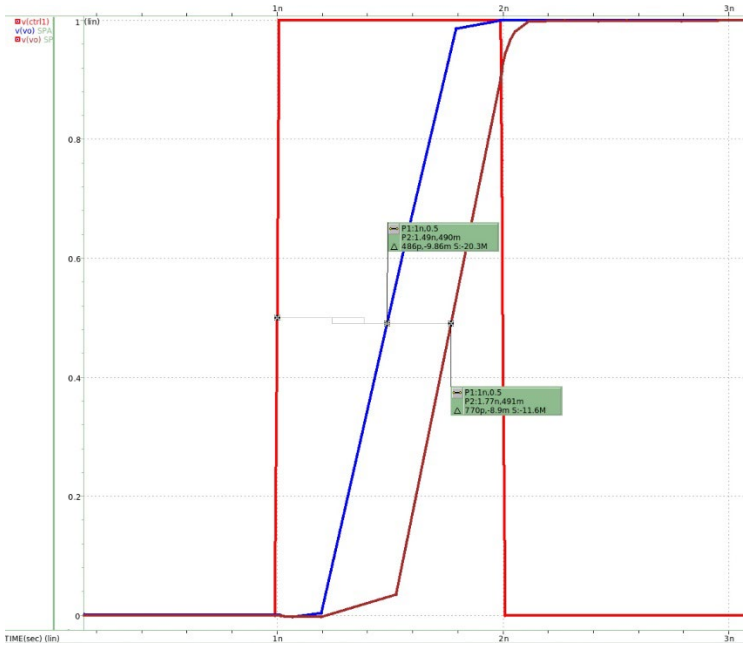

Fig. 7 The sensitivity of PMOS M12

4.2 PCB Measurement Results

From Fig. 8 and Fig. 9, it can be observed that the IC component (MC74AC14: Hex Inverter Schmitt Trigger) exhibits excessively long fall time and rise time. As a result, the measurement method described in the previous section is unable to accurately capture the actual dead time of the circuit, and the true waveform characteristics cannot be clearly observed. This issue indicates that more suitable IC

components must be selected to properly resolve the problem. Fig. 10 is the PCB layout design of the circuit

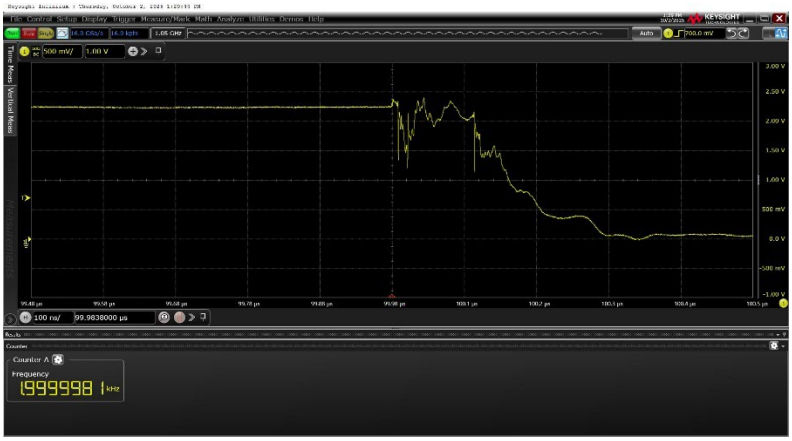

Fig. 8 Fall Time of the MC74AC14 Hex Inverter Schmitt Trigger

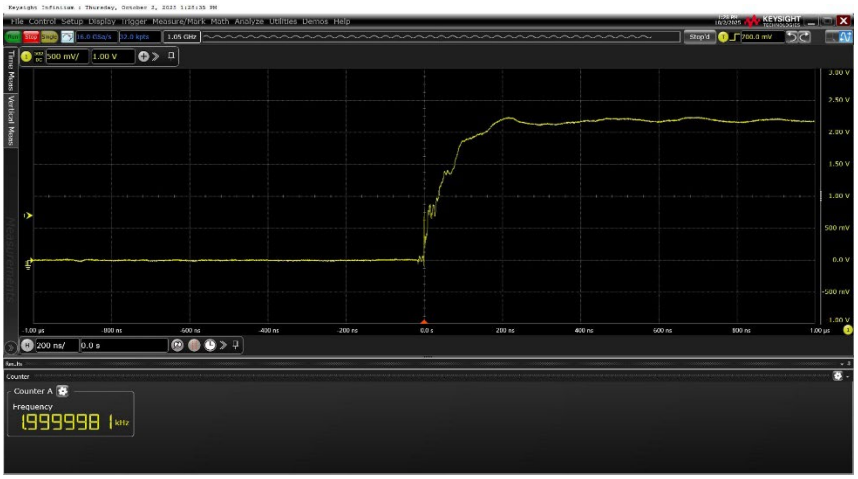

Fig. 9 Rise Time of the MC74AC14 Hex Inverter Schmitt Trigger

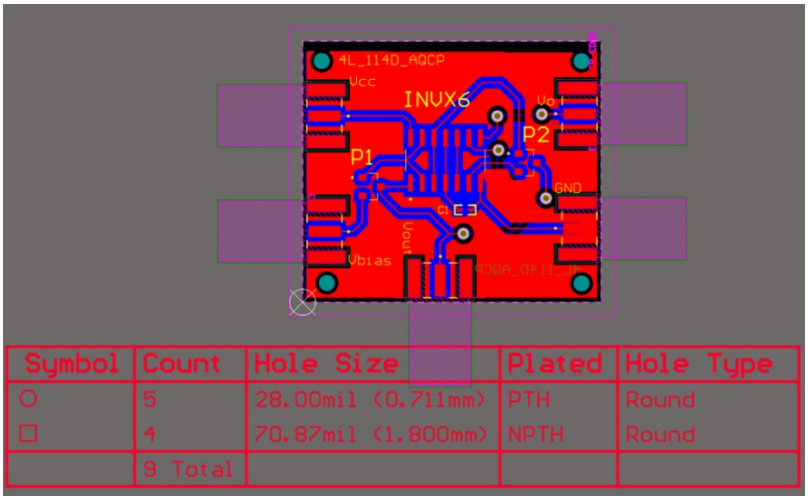

Fig. 10 PCB layout of AQC

5. Conclusion

This work presents the design and validation of an external active quenching circuit (AQC) for SPAD-based single-photon detection. After reviewing key performance metrics such as PDE, DCR, dead time, and afterpulsing, as well as the limitations of passive and active quenching schemes, an improved AQC architecture is implemented featuring a low-latency comparator and a fast recovery path. The proposed design is evaluated through circuit-level simulations and PCB-based measurements. $R_{ds(on)}$

Simulation results confirm that the AQC significantly reduces recovery time and provides a stable buffered output suitable for system integration. Compared with passive quenching, architecture offers better efficiency and tunability, making it promising for applications such as 3D imaging and quantum communication. However, measurement results were affected by the large $R_{ds(on)}$ of the selected PMOS and the intrinsic delay of the IC components, which reduced avalanche detection sensitivity and impacted the observed circuit behavior.

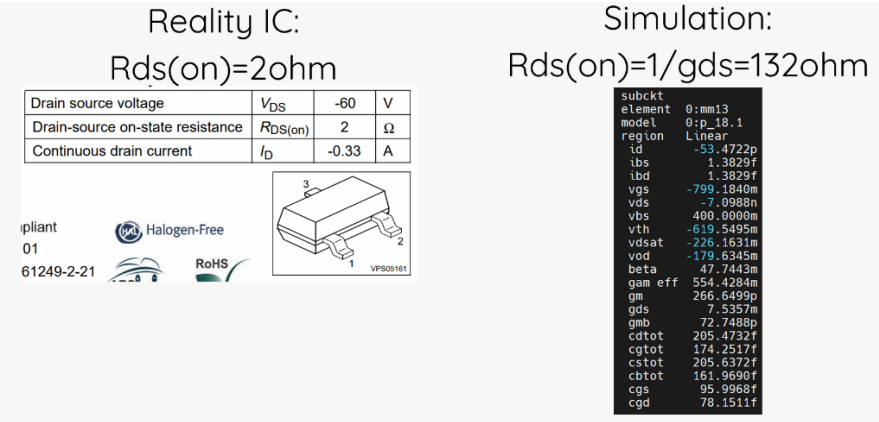

Fig. 11 Actual vs. Simulated PMOS $R_{ds(on)}$

The measured $R_{ds(on)}$ of the purchased PMOS is significantly larger than the value assumed in simulation, requiring the breakdown pulse to be amplified to about 0.01 A for proper circuit response—roughly two orders of magnitude greater than a real SPAD avalanche current. This discrepancy indicates the need for further refinement. Future improvements include selecting IC components with more appropriate $R_{ds(on)}$, addressing issues such as delay, waveform distortion, and biasing, and potentially reducing circuit area or adding features such as adjustable hold-off control. Developing a more accurate SPAD equivalent model and extending the design to multi-channel or array architectures would also enhance system

scalability. Overall, the results confirm the feasibility of the improved AQC and provide a practical reference for advancing SPAD detector performance.

Fig. 12 Actual PMOS with Larger Drain–Source Resistance

6. Reference

[1] 許宏任, "Single-Photon Avalanche Diode Controlled by Active Quenching Circuit" 臺灣博碩士論文加值系統, 2011

7. Review and Reflection

在這次設計淬火電路的專題中，我們一開始從熟悉的領域著手，運用部分課程中的模擬與電路分析能力逐步優化架構；接著踏入完全陌生的範疇，從 PCB layout、元件挑選，到最終的焊接與實際量測。雖然最後成功把電路做出來，但量測結果也清楚揭示了許多尚未掌握的細節，有些問題甚至在事後才懊惱當初沒有提前注意。 然而，這些不足與挫折反而是最寶貴的學習經驗。透過完整走過設計、佈局到實作的流程，我們不僅對 PCB layout 的步驟有更深刻的理解，也在量測過程中逐步培養了分析訊號、判斷問題來源，以及推理電路行為的能力。這些過程讓我們建立起「面對問題、拆解問題、解決問題」的實作能力。 更重要的是，這次專題讓我們真正體會到如何把課堂所學套用到實際情境中。無論是 SPICE 模擬、器件選型、佈局考量，還是訊號分析，我們把理論轉化為能直接應用的技能。希望這些經驗能讓我們在未來更複雜的專題與研究中運用所學解決問題，並在每一次實作中持續成長。