Measurement and Analysis of Anti-Fuse Memory Cell

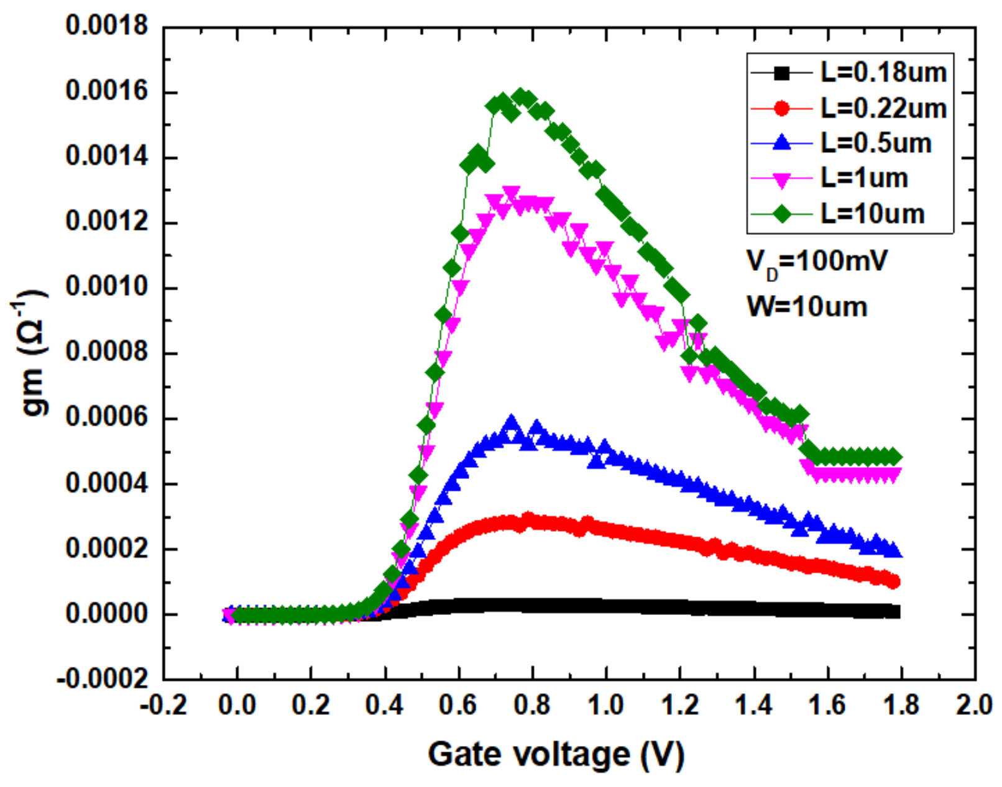
Group: A395 Members : 何明蔚、陳仕瑜 Supervisor : 金雅琴 教授

ABSTRACT

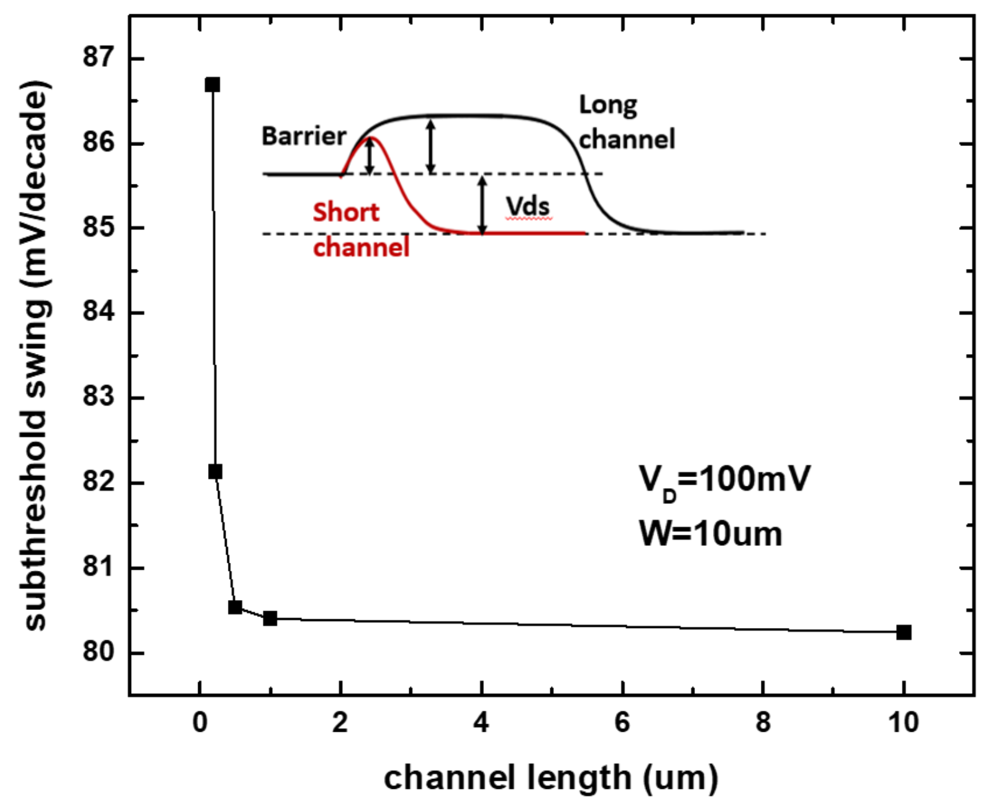
One-Time Programmable (OTP) memory is widely used for permanently storing data, and it finds application in various electronic products. Our research first introduces the basic NMOS characteristics and its geometric effect. Then, our research presents measurement results and analysis of an anti-fuse memory cell. Through electrical analysis, the anti-fuse cell exhibits characteristics such as rapid programming, high read window, and independence of program operations. Furthermore, we analyze the performance of memory arrays, conducting read disturb tests on the anti-fuse cell array, which demonstrates extremely high read current difference and excellent reliability.

NMOS MEASUREMENT & ANALYSIS

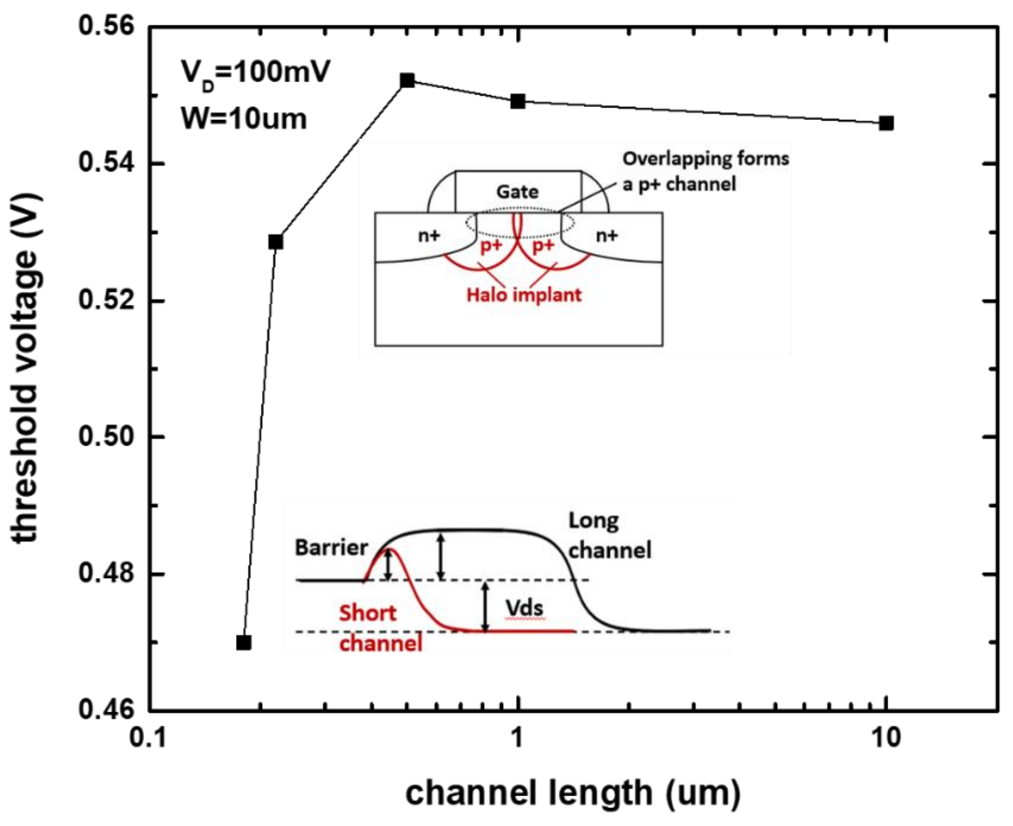
To find Vth of 5 different channel length NMOS, we use gm maximum method. The gm-V_G curve is in Fig.1 , for V_{TH} extraction. V_{TH} of different length is shown in Fig.2 For channel length < 5µm, V_{TH} drops sharply as length becomes smaller due to short channel effect. For channel length > 5µm, V_{TH} is mainly affected by halo implant overlap. Subthreshold swing is obtained from the equation below. Shown in Fig.3 , subthreshold swing is higher for short channel.Fig.4 shows the relation between I_D and L^{-1} , considering channel length modulation, we divide I_D by a factor of $(1+\lambda V_D)$. After dividing, the result is more proportional to L^{-1}.



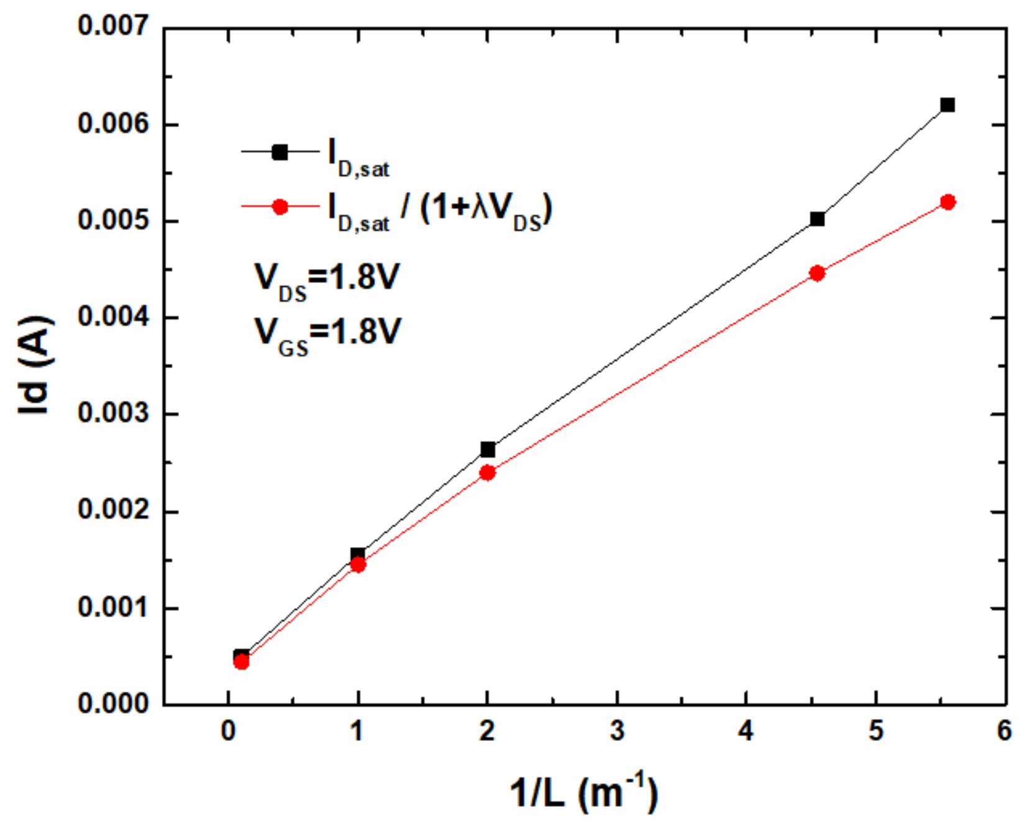
← Fig.1



← Fig.3

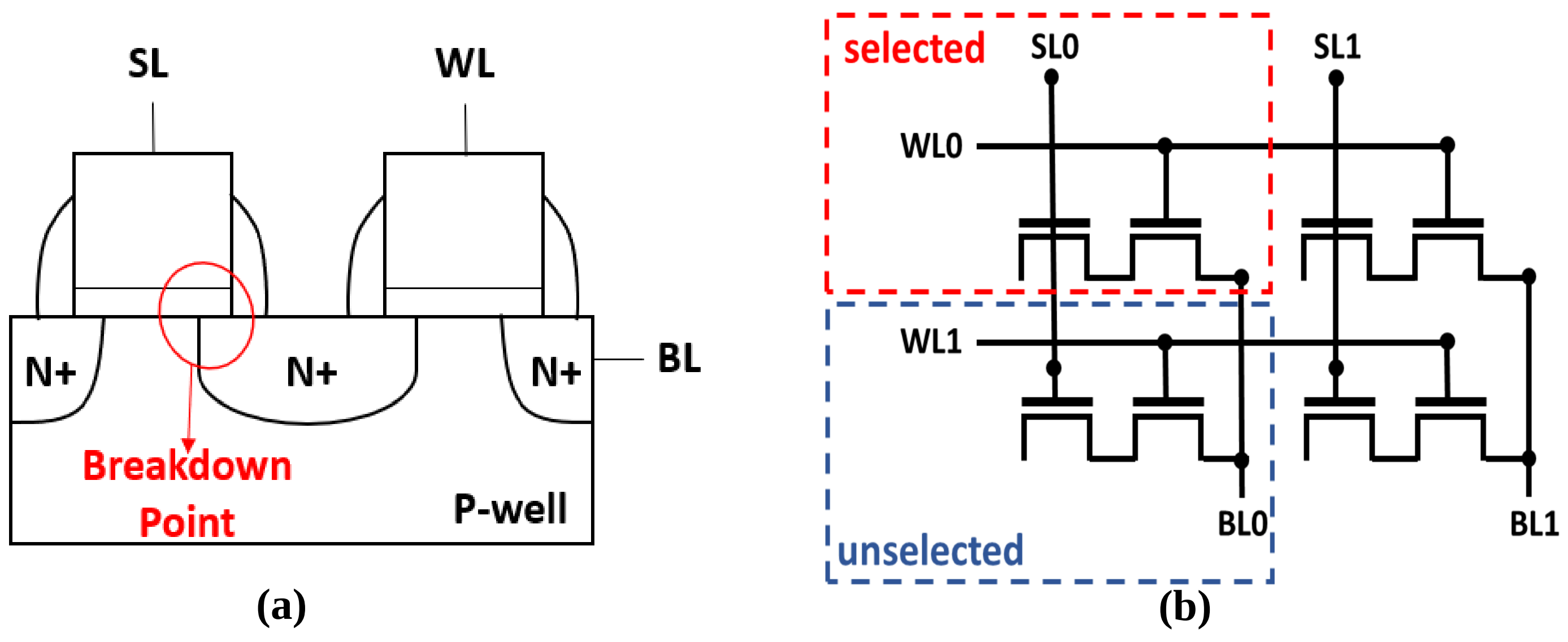


← Fig.2



← Fig.4

ANTI-FUSE CELL STRUCTURE



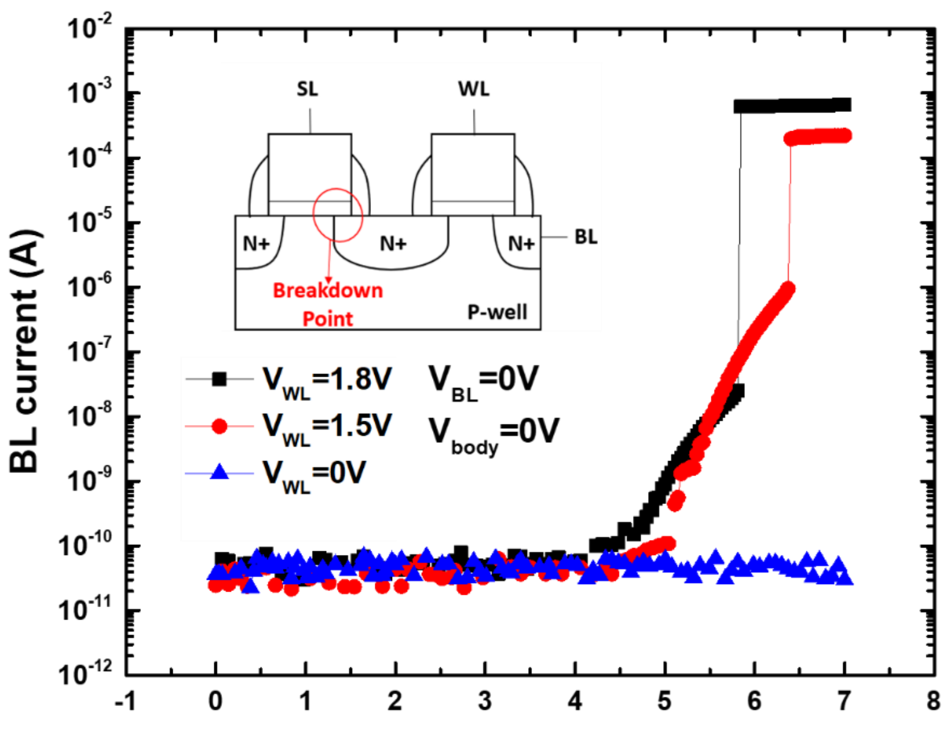
(a) (b)

Fig.5

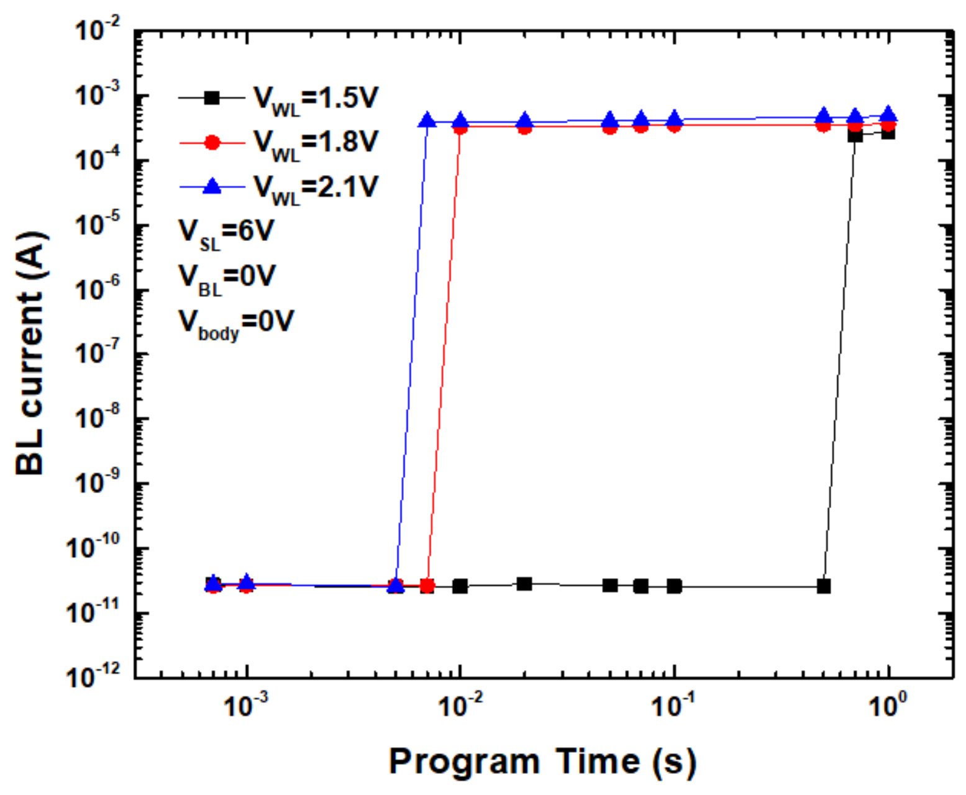
The Anti-Fuse cell we measured is constructed by two NMOS in series as in Fig.5(a), as programmed, oxide layer breakdown happens between the SL and the n+ diffusion. For oxide to breakdown, high voltage differences across the oxide is set by V_{WL}=1.8V and V_{BL}=0V, so that n+ region is 0V, then we apply high voltage on SL. In an Anti-Fuse array in Fig.5(b), WL is for selection. When reading the Anti-Fuse cell, we let $V_{SL}=V_{WL}$=1.8V, V_{BL}=0V. If the cell is programmed, I_{BL} will be high. If not, I_{BL} remains low.

ANTI-FUSE CELL MEASUREMENT & ANALYSIS

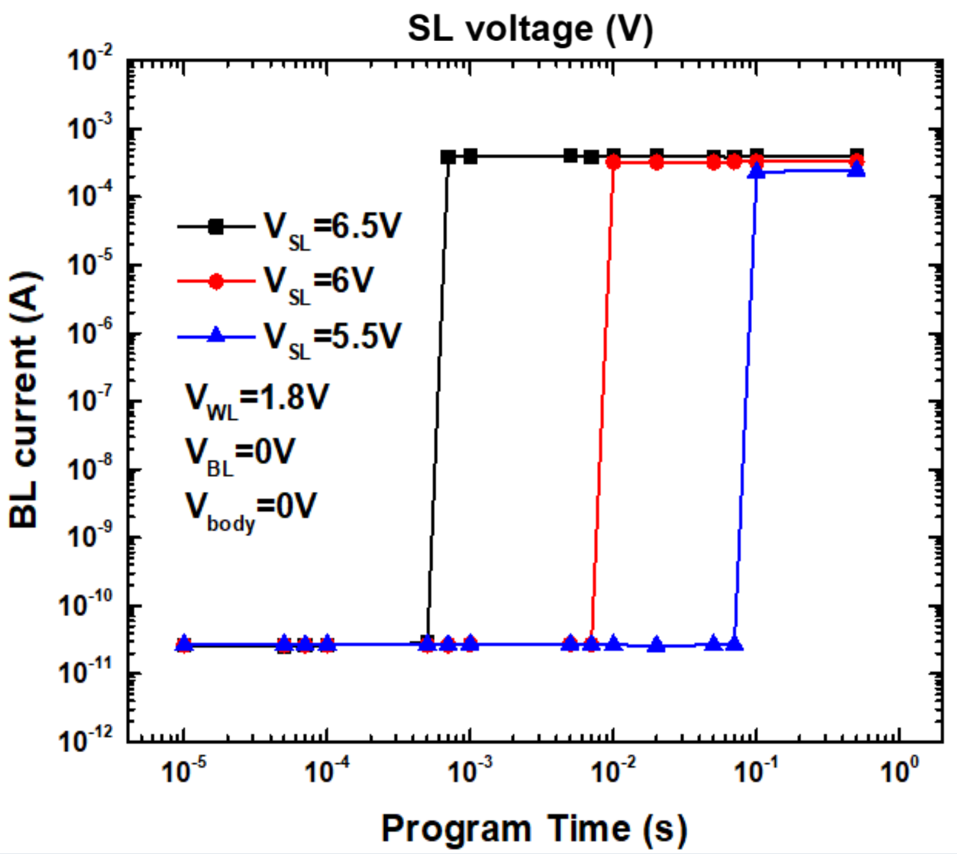
Higher WL voltage makes oxide breakdown happen at lower SL voltage, as Fig.6 shows. As larger voltage applied on SL, the voltage and the electric field crossing the oxide of SL become larger, leading to faster program speed and larger BL current. In Fig.7, SL voltage shows the ability to control program speed. As Fig.8 shows, the program speed is faster when applying larger WL voltage. As SL voltage increases, the difference between BL current of the selected cell and that of the unselected cell becomes larger. WL controls which cell to be read, see Fig.9 .



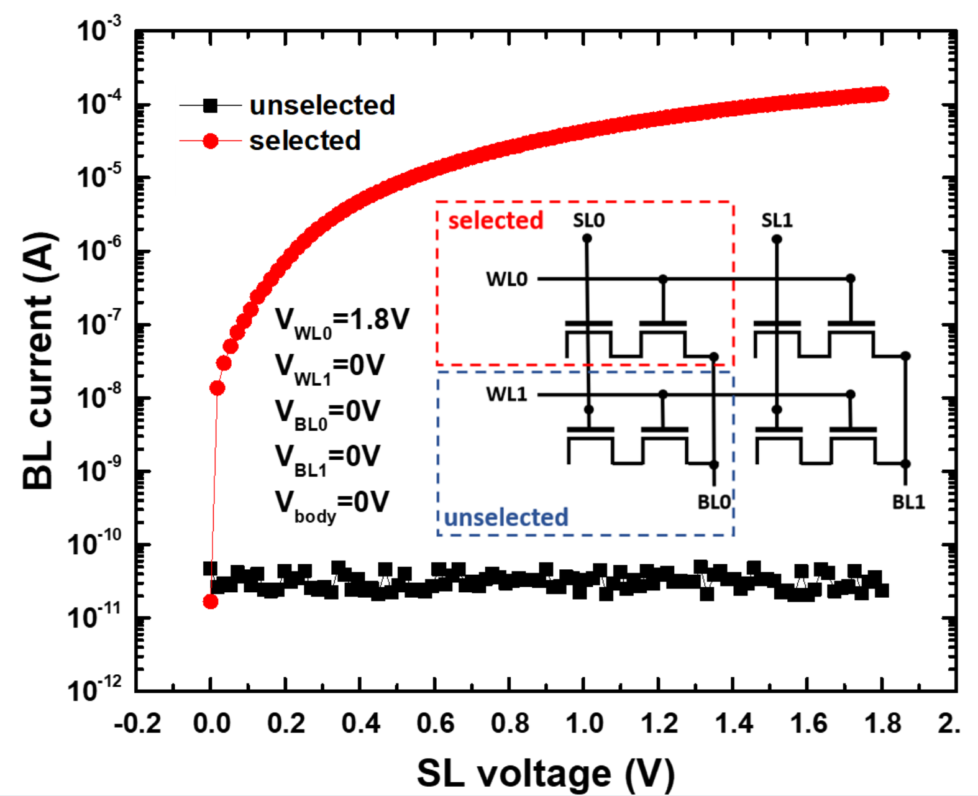
← Fig.6



← Fig.8



← Fig.7



← Fig.9

CONCLUSION

This project delves into the various electrical performances of both basic NMOS and Anti-Fuse Cells. Observations of V_{TH} Roll Off caused by Short Channel Effect and V_{TH} rise due to Halo Implant. We then conducted deeper measurements on Anti-Fuse Cells. Firstly, we study the V_{WL} and V_{SL} effects on its operations. Subsequently, the cells are programmed by different V_{SL} and V_{WL} pulses and found that larger V_{SL} and V_{WL} corresponded to faster program speed and higher instantaneous breakdown currents. Finally, we further discussed the Anti-Fuse Array. Besides achieving good Program Inhibit characteristics by changing V_{WL}, optimal read condition is investigated.