國立清華大學 電機工程學系

實作專題研究成果報告

Design and analysis of high-gain CMOS low-noise amplifiers for 5G communications

適用於5G 行動通訊之 CMOS 高增益低雜訊放大器設計與分析

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Abstract

This paper presents different structures of single-end (SE) 28 GHz low-noise amplifier (LNA) for 5G applications. The proposed 2-stage low-noise amplifier (LNA) with both stages implemented using common-source (CS) topology reaches a measured gain of 19.2 dB, a 3-dB bandwidth from 25.4 to 30.6 GHz, and a noise figure (NF) of 3.6 dB. When the second stage is replaced by a cascode topology, the measured gain increases to 20.6 dB, with a 3-dB bandwidth ranging from 25.7 to 30.4 GHz without changing NF.

For the 3-stage LNA, where the first two stages adopt CS topology, the configuration with a CS third stage reaches a measured gain of 27.9 dB, a 3-dB bandwidth from 25.8 to 30.1 GHz with the same NF of the 2-stage LNA. Changing the third stage with a cascode configuration improves the gain to 29.2 dB, with a 3-dB bandwidth from 26.1 to 29.8 GHz, while maintaining the NF of 3.6 dB. All designs are implemented using TSMC’s 90 nm RF CMOS process.

摘要

本文探討多種應用於第五代行動通訊（5G）之單端（Single-Ended, SE）28 GHz 低雜訊放大器（Low-Noise Amplifier, LNA）架構設計。其中所提出之二級放大器架構中，兩級皆採用共源極（Common-Source, CS）拓撲實現，其量測增益達 19.2 dB，對應之 3 dB 頻寬範圍為 25.4 至 30.6 GHz，雜訊指數（Noise Figure, NF）為 3.6 dB。若將第二級改為 cascode 拓撲，則增益將提升至 20.6 dB，3 dB 頻寬為 25.7 至 30.4 GHz，而其雜訊指數維持不變。

針對三級放大器架構，本文前兩級皆採用共源極 CS 拓撲。當第三級為共源極 CS 結構時，量測增益為 27.9 dB，3 dB 頻寬涵蓋 25.8 至 30.1 GHz，雜訊指數與前述二級架構相同。若將第三級改為 cascode 拓撲，則可將增益進一步提升至 29.2 dB，對應之 3 dB 頻寬範圍為 26.1 至 29.8 GHz，且噪聲指數仍維持於 3.6 dB。上述所有電路設計均以 TSMC 90 nm RF CMOS 製程實現。

1. Introduction

In recent years, the development of fifth-generation wireless systems (5G) has rapidly advanced, offering significant improvements in terms of data rates, latency, and large-scale device connectivity. To meet the demands for high data throughput and high resolution in emerging applications the millimeter-wave (mm Wave) band has been adopted. The 24–29 GHz frequency range is among the most widely adopted for 5G applications [1]. Accordingly, we choose to operate at 28 GHz in this work.

The low-noise amplifier (LNA) is the initial active component in a receiver, which affects the overall sensitivity of the system and noise performance [2]. A high gain in the LNA stage not only amplifies the RF received signal but also reduces the impact of its noise contribution on the whole receiver chain, as described by the Friis formula [3].

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \qquad (1)$$

The CS stage is widely adopted due to high gain and good noise performance, which can be improved by adding inductors at the sources of the transistors (source degeneration) to reduce the noise figure (NF) and enhance the stability of the CS stages [4].

A wideband input impedance matching architecture was presented in [5]. Two common-gate (CG) transistors are employed in a current-reuse configuration, with one of the CG transistors is positioned above the other to present a parallel configurations at the input. This technique reduces the required input transconductance by half compared to a basic CG LNA without affecting the overall gain of each NMOS transistor. Likewise, positive feedback is utilized in an LNA design to effectively cancel the noise generated by the input CG transistor [7]. In this work, we focus on two widely used transistor configurations in CMOS LNA: the common-source (CS) and cascode configurations [2].

2. Purpose

By comparing these two configurations, this paper presents two two-stage LNA and two three-stage LNA. In this work, the mm-wave LNA are designed and simulated multi-stage LNA topologies in ADS with TSMC 90nm RF CMOS PDK.

3. Method

3-1 Proposed LNA Architecture

3-1.1 Two Stages

3-1.1.1 Common Source + Common Source

The common-source (CS) configuration is widely used in CMOS low-noise amplifiers (LNAs) due to its high voltage gain and favorable noise performance. CS configuration may be used in wideband applications using special feedback or matching circuits [6]. Moreover, thanks to its substantial gain and moderate input impedance, the CS stage is commonly employed as the first amplification stage. Its relatively simple structure—typically requiring only a single transistor—further contributes to its popularity in integrated circuit design.

A CS topology connected to inductor source-degeneration. This structure is conventionally applied in narrowband LNA designs but can be extended to wideband applications using feedback or advanced matching techniques [6]. The CS topology with inductive source-degeneration technique is popularly used in LNA designs, due to its advantage of simultaneous input conjugate impedance and noise matching [4].

The source inductor can suppress the channel thermal noise of the CS transistor so that it can improve the overall noise performance. However, compared to the CS topology without source inductor, the gain will decrease, and the chip area will also increase.

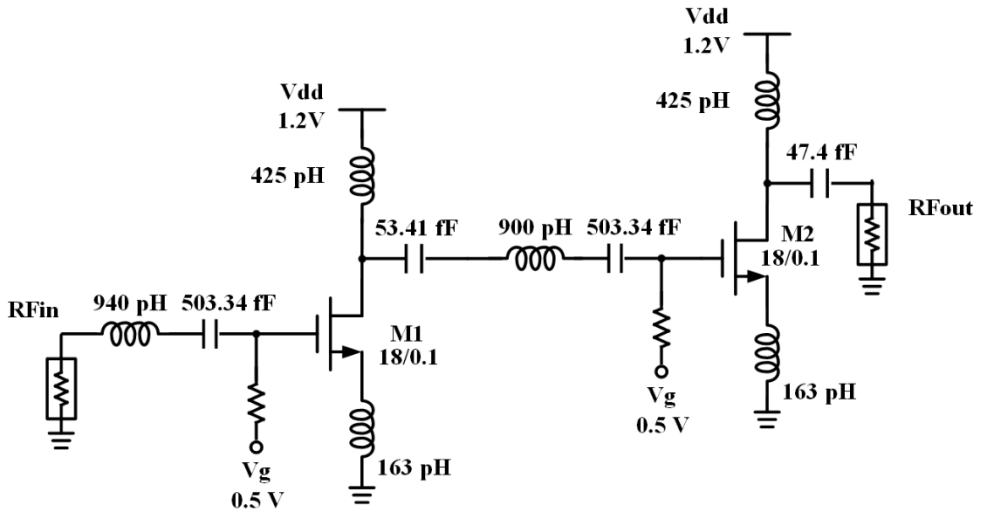

Fig. 1 the proposed 28-GHz two-stage CS + CS LNA schematic

The LNA cascades two stages to give enough gain at Ka-band. The first stage, which consists of the CS topology with source inductor, mainly determines the noise of the whole structure. The transistor size of 18 μm is selected to have minimum noise figure NF_{min} and maximum gain. Moreover, to achieve input impedance matching, an inductor and a cascade capacitance are utilized to adjust input impedance Z_{in} and the complex conjugation of the optimal noise impedance to be close to 50 Ω. The drain inductor is used to resonate out the parasitic capacitance at the M_1 drain to boost the gain at frequency of interest [7]. However, the gain of the first stage is not enough to meet the specification. Consequently, we apply the second stage. The topology of the second stage should also have low-noise performance so that we add the second with the same structure, then the NF changes from 3.339 dB to 3.588

dB, which does not increase a lot compared to the gain changes from 9.498 dB to 19.121 dB that is more than two times. And the inductors and the capacitances are used to match between two transistors.

3-1.1.2 Common Source + Cascode

The cascode configuration provides high power gain, favorable noise performance, low power consumption and high reverse isolation [8]. At lower microwave frequencies, the noise from the upper transistor of the cascode transistor is effectively suppressed by the output impedance of the common-source configuration [11]. However, as the operating frequency increases, the excellent noise and performance gain of the cascode configuration decreases. This degradation is primarily caused by increasing substrate parasitic admittance at the shared drain-source node [8], which lowers the impedance seen at the source of the upper transistor and makes its drain noise to appear at the output term. Like the CS topology, the cascode configuration is inherently suitable for narrowband designs. Nevertheless, it can be extended for multi-band or wideband applications with more complex LC-based matching networks in the input [12].

To overcome the limitation of using the cascode configuration in the first stage due to its degraded noise performance at high frequencies, two design approaches have been proposed. The one of them employs a resonant network to cancel the junction capacitance of the cascode transistor, as presented in [13]. The other adopted in the work utilizes a single transistor amplifier in the first stage to remove the noise generated by the cascode device, while a cascode configuration is employed in the second stage to enhance gain.[13] Fig. 2 illustrates the schematic of the proposed 28-GHz LNA, designed and simulated in ADS using TSMC 90-nm CMOS PDK components. All inductors are modeled using high-Q INDQ elements, which are optimized for operation at millimeter-wave frequencies. Capacitors are selected from the PDK device set to ensure realistic performance modeling during simulation.

To achieve simultaneous noise and impedance matching (SNIM) in the two stages LNA, a source degeneration inductor of M1 and M2 in Fig.2 and output L-type matching network are employed to align the input impedance Z_{in} with the complex conjugate of the optimum noise impedance Z_{opt}, matching near 50Ω. And the simulated S11 and S22 around the center of the Smith chart at 28 GHz, the SNIM is achieved.

In order to improve the gain at the operating frequency, an inductor is used at the drain of M1 to resonate out its parasitic capacitance.[7] The first stage is mainly designed for minimal noise figure (NF), which results in limited gain. Therefore, the second stage adopts a cascode configuration to achieve higher gain while maintaining acceptable overall noise performance.

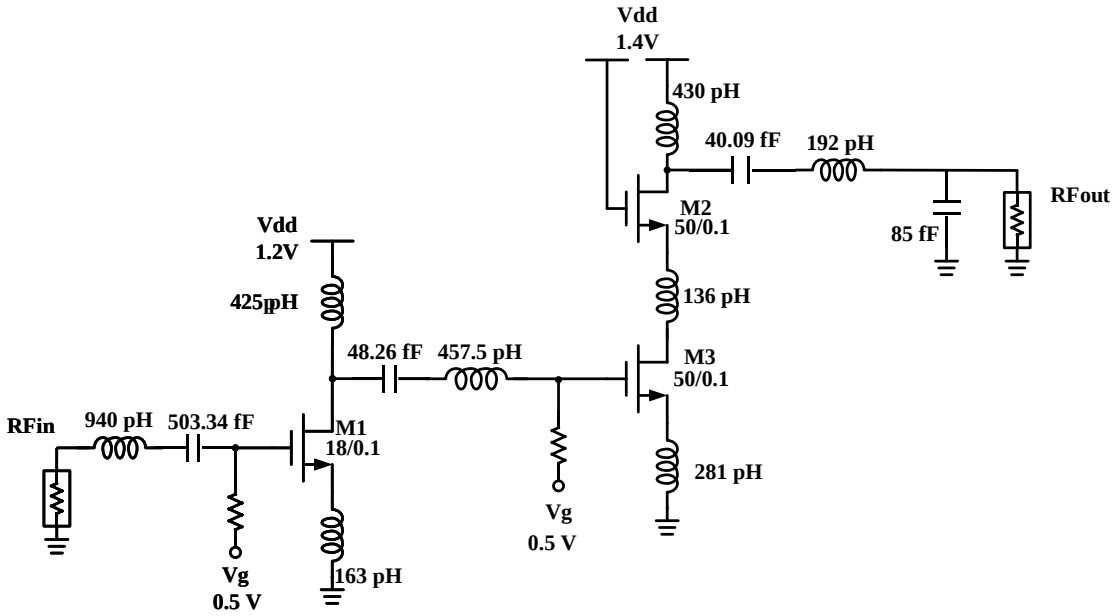

Fig. 2 the proposed 28-GHz two-stage Common Source + Cascode LNA schematic

To analyze the impact of supply voltage on circuit performance, V_{DD} was swept from 1.2 V to 1.6 V. The minimum noise figure (NF_{min}) and the overall noise figure exhibit a slight decreasing trend as V_{DD} increases, suggesting a slight improvement in noise performance.

The gain increases more significantly with higher V_{DD}, especially over 1.45 V, due to improved headroom and increased output swing. This verifies that a higher supply voltage can improve the gain characteristics of the LNA. The stability parameters, Mu-factor and the stability K-factor, both slightly decrease as V_{DD} increases but remain well above the unconditional stability threshold across the entire sweeping range, indicating acceptable stability even under higher bias conditions.

In addition to gain and noise performance, increasing V_{DD} also provides more voltage headroom for the transistors, which can improve linearity by reducing distortion under large-signal conditions. However, this comes at the cost of increased power consumption, as the total dc power dissipation scales with the supply voltage. Therefore, there exists a trade-off between improved performance and power efficiency that must be considered when selecting the optimal V_{DD}. In our design, $V_{DD} = 1.4$ was selected as the operating point, as it provides a balanced trade-off among gain, noise figure, and stability, while maintaining reasonable power consumption. Furthermore, this bias condition favors input and output matching, ensuring efficient power transfer and minimizing reflection losses across the operating frequency.

3-1.2 Three Stages

3-1.2.1 Common Source + Common Source+ Common Source

The proposed three-stage LNA is implemented by replicating a single-stage common-source (CS) amplifier with small adaptations for each stage. The first CS stage is designed

with an output L-type matching network, consisting of a series capacitor that couples to the next stage and a series inductor connected to AC ground. This matching scheme is extended to subsequent stages to maintain design consistency and simplify implementation. Inter-stage matching is achieved through a combination of the previous stage's output L-type network and a series LC network at the gate of the next stage, allowing for efficient power transfer and effective impedance transformation [14].

All three stages adopt the common-source topology with source degeneration inductors, which not only support local input matching but also improve linearity by limiting the voltage swing at the source terminals. This modular design method enables straightforward scaling, predictable performance, and improves control over bandwidth and gain [15].

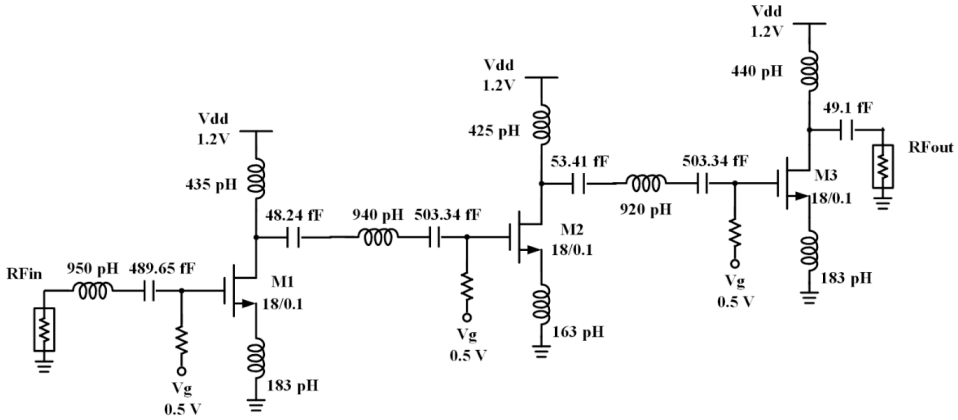

Fig. 3 the proposed 28-GHz two-stage CS + CS + CS LNA schematic

3-1.2.2 Common Source + Common Source + Cascode

In this three-stage LNA, the first stage employs the same common-source (CS) amplifier circuit as developed in the initial single-stage prototype. This stage provides low noise and sufficient gain, forming a reliable foundation for the subsequent stages. To further enhance performance, the second and third stages adopt the CS-Cascode topology described in Section 2-1.2, which improves gain, bandwidth, and reverse isolation.

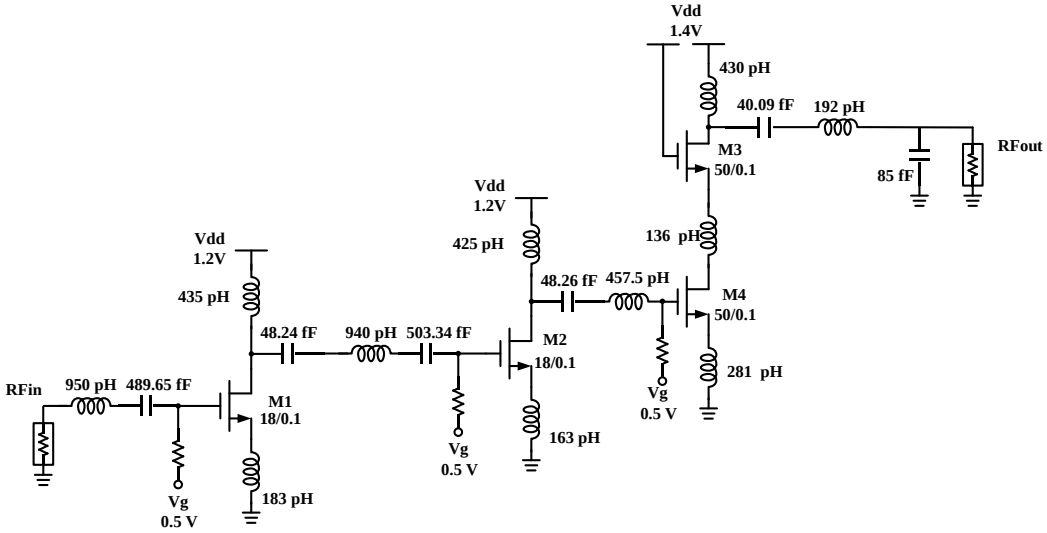

Fig. 4 the proposed 28-GHz two-stage CS + CS + Cascode LNA schematic

Although mathematical treatment such as equations (2) and (3) [14] offer a means to estimate optimal noise and impedance conditions, they depend heavily on exact values of parasitic components, such as the load inductor L_D, which are often difficult to predict in practice.

$$Z_{o1} = \sqrt{\frac{L_M}{C_{gs2}+C_{sb2}}} = Z_{Q1,load} \quad (2)$$

$$Z_{o1} = Z_{Q2,in} = \frac{1}{g_{m2}} + \frac{\omega L_M Q}{1+g_{m2}r_{02}} \quad (3)$$

Due to such limitations, a Smith chart-based design approach is adopted to determine the input impedance that satisfies both noise and power matching for the transistors used. For efficient signal transfer, inter-stage matching networks are implemented.

Fig. 4 illustrates the third-stage cascode topology. A series inductor L_M is inserted between the common-source and common-gate transistors to compensate for the mid-band pole introduced by the cascode topology. In combination with the transistors intrinsic capacitances (such as C_{gs}, C_{sb}, C_{db}, and C_{gd}), L_M forms an artificial transmission line that improves impedance matching, increases the transition frequency f_T, and extends bandwidth for millimeter-wave operation.

3-2 Gain Analysis

The CS–CS topology provides approximately 9.51 dB gain from the first stage and 9.54 dB from the second stage, resulting in a total gain of 19.1 dB at 28 GHz. This configuration has low circuit complexity and consistent noise performance. However, its gain is inherently limited, which may limit its applicability in high-gain systems.

When the second stage is replaced with a cascode structure (CS–cascode), the gain from the first stage remains approximately 9.50 dB, while the cascode second stage contributes 11.05 dB, yielding a total gain of 20.6 dB. This arrangement offers improved gain

performance relative to CS–CS while maintaining low overall design complexity. The cascode topology can be viewed as an integrated two-transistor arrangement consisting of a common-source stage cascaded with a common-gate stage. This configuration effectively functions as a two-stage amplifier, offering enhanced bandwidth and reverse isolation without resulting in significant area overhead.

The CS–CS–CS topology has uniform gain distribution across all three stages, with stage gains of 9.15 dB, 9.50 dB, and 9.18 dB respectively, resulting in a total gain of 27.9 dB at 28 GHz, as shown in Fig. 14. This confirms effective inter-stage matching and stable gain contribution per stage. However, this topology may exhibit bandwidth and stability limitations due to the increased Miller effect in the final stage. In the earlier stages, the gate-drain capacitance (C_{gd}) is partially attenuated by the input impedance of the subsequent stage. In contrast, the final stage directly drives the output network, and the absence of a subsequent stage prevents mitigation of the Miller multiplication effect. The larger voltage swing at the output further amplifies this effect. Without sufficient source degeneration or robust output matching, this can lead to undesired feedback and reduced stability under high-frequency operation.

The CS–CS–cascode configuration, where the final stage employs a cascode structure, achieves the highest total gain of 29.4 dB. The first and second stages contribute 9.15 dB and 9.50 dB, respectively, while the third-stage cascode adds 11.05 dB. The enhanced performance of the third stage is due to the increased output impedance and improved isolation from the load, which are characteristic advantages of cascode topology. This design provides high gain while maintaining frequency-domain robustness and a manageable design footprint.

These results underscore the trade-offs in multi-stage LNA design with respect to gain, noise, linearity, and implementation complexity. The CS–CS–cascode topology offers the highest gain and good high-frequency behavior, but it necessitates bias control and layout planning. The CS–CS–CS design supports consistent gain stacking and simple implementation but may be less suitable for wideband or highly linear applications [7]. The CS–cascode architecture offers moderate gain enhancement with minimal complexity overhead. The CS–CS topology is limited in gain, which provides the simplest design and lowest power consumption, making it suitable for low-power systems with relaxed performance requirements.

3-3 Noise Analysis

The noise figure (NF) of the low-noise amplifier (LNA) has a direct impact on the overall noise performance of the receiver that it would directly add to that of the receiver. Consequently, the NF of the LNA is typically designed to be about 2 to 3 dB. Refer to [4], the expressions for the channel thermal noise ($\overline{\iota_{dı,n}^2}$) and the thermal noise due to parasitic resistances ($\overline{\iota_{gı,n}^2}$) of the MOS transistors are given by :

$$\overline{i_{d\iota,n}^2} = 4kT(\frac{\gamma_i}{a_i})g_{mi}\Delta f \quad (4)$$

$$\overline{i_{g1,n}^2} = 4kT(r_{gi})^{-1}\Delta f \quad (5)$$

, where $a_i = g_{mi}/g_{d0i}$. Also, by the equation and by Friis formula, we can realize that the first stage dominates the NF of the whole LNA.

4. Simulation Results

4-1 Two Stages

4-1.1 Common Source + Common Source

The simulated S-parameters of the proposed two-stage amplifier. It can be observed that both the input reflection coefficient (S11) and the output reflection coefficient (S22) are below –20 dB at the frequency of 28 GHz, indicating good impedance matching at both the input and output ports. Such matching is critical for maximizing power transfer and minimizing signal reflection in high-frequency applications.

The forward transmission coefficient S21 reaches 19.224 dB at 28 GHz, and the corresponding 3-dB bandwidth is measured to be 5.24 GHz. At the design frequency of 28 GHz, the NF is 3.588 dB while the NF_{min} is 2.943 dB, indicating near-optimal noise performance with minimal degradation due to input mismatch. And the fundamental and third-order components were extrapolated using linear regression to estimate the input-referred third-order intercept point (IIP3), which is calculated to be –7.822 dBm. This value reflects moderate linearity, which is acceptable for low-power RF front-end applications where noise performance is prioritized.

4-1.2 Common Source + Cascode

The CS+Cascode topology was designed to balance gain, noise, and linearity. The S-parameter simulation illustrates that the circuit achieves a power gain (S21) of approximately 20.6 dB at 28 GHz, with a −3 dB bandwidth of 4.7 GHz. The gain remains flat across a wide frequency range, confirming the broadband behavior of this configuration. Noise performance was evaluated using the simulated minimum noise figure (NF_{min}) and the actual noise figure under optimal source matching. The noise figure remains low at 3.59 dB, which satisfies the target of below 4.5 dB. Linearity was assessed through a two-tone test yielding an OIP3 of 5.89 dBm and OP_{1dB} of −2.18 dBm. The IIP3 was extracted as −15.34 dBm. And the input-output power transfer curve is used to extract the IP_{1dB}, which occurs at −25.4 dBm input power. Overall, this topology offers a moderate gain and linearity with acceptable power consumption.

4-2. Three Stages

4-2.1 Common Source + Common Source + Common Source

The CS+CS+CS topology was developed to maximize gain while maintaining acceptable noise and linearity. In the S-parameter simulation, it achieves a gain of 27.86 dB at 28 GHz, with a −3 dB bandwidth of 4.3 GHz. The gain enhancement is attributed to the cumulative amplification across three common-source stages. And a measured NF of 3.63 dB, which is still well below the specification limit. Linearity performance, analyzed via the two-tone test, demonstrates an OIP3 of 11.15 dBm and an OP_{1dB} of −0.29 dBm. The IIP3 is −17.20 dBm, indicating robust linearity compared to the previous topology. The IP_{1dB} occurs at −26.3 dBm input level, confirming good compression characteristics. This topology offers the best performance gain among the three, with reasonable linearity and a power consumption of 11.14 mW.

4-2.2 Common Source + Common Source + Cascode

The CS+CS+Cascode topology integrates a cascode stage at the output to improve isolation and gain stability. According to the S-parameter results, the circuit achieves a high gain of 29.19 dB at 28 GHz, with a −3 dB bandwidth of 3.7 GHz. While the bandwidth is slightly narrower than the other topologies, the gain is the highest among the three. The noise figure remains low at 3.63 dB, confirming compliance with design requirements. In the two-tone linearity test, from which an OIP3 of 6.16 dBm and OP_{1dB} of −2.28 dBm were extracted. However, the IIP3 is relatively low at −25.71 dBm, indicating reduced linearity tolerance at high input powers. The input-output curve shows that the IP_{1dB} occurs at −35.0 dBm, the lowest among the tested topologies. While this design achieves the highest gain, it trades off linearity and consumes the most power at 15.46 mW.

Table 1

Performance Summary and Comparison

Ref.	CMOS Process	Freq. (GHz)	Gain (dB)	NF (dB)	BW (GHz)	OP_{1dB} (dBm)	OIP3 (dBm)	IP_{1dB} (dBm)	IIP3 (dBm)	P_{DC} (mW)	Topology
[9]	65nm	28	18.2	3.9-4.1	12	--	--	-15	--	9.8	CS+CS
[7]	90nm	35	45.2	4.7	3.4	--	--	-64	--	29.9	CS+Cascode
[1]	90nm	28	15.8-18.8	2.3-4.2	--	--	--	--	--	3.7-4.5	CS+Cascode
[13]	90nm	28.5	20	2.9	2.6	2	12.5	--	--	--	CS+Cascode
[14]	90nm	58	14.6	<5.5	--	--	--	--	-6.8	24	CS+CS+CS
[16]	90nm	57	18.6	5.7	--	--	--	-14.8	--	29	CS+CS+CS
Spec	90 nm	28	>15	<4.5	3	--	--	-40	-30	10~15	--
This work			19.224	3.588	5.24	5.61	11.5	-18.4	-7.822	6.36	CS+CS
			20.631	3.594	4.7	-2.18	5.89	-25.4	-15.338	12.77	CS+Cascode
			27.858	3.627	4.3	-0.29	11.15	-26.3	-17.195	11.14	CS+CS+CS
			29.191	3.63	3.7	-2.28	6.16	-35.0	-25.705	15.46	CS+CS+Cascode

5. Conclusion

This work presents a study of various single-ended (SE) 28 GHz low-noise amplifier (LNA) architectures for 5G applications, implemented using TSMC's 90 nm RF CMOS process. The measured results demonstrate that the choice of using cascode would increase the gain. As mentioned, the two-stage common-source (CS) LNA achieves a gain of 19.2 dB with a 3-dB bandwidth of 25.4–30.6 GHz and a noise figure (NF) of 3.6 dB. Replacing the second stage with a cascode configuration improves the gain to 20.6 dB while maintaining a similar bandwidth and noise performance.

Furthermore, the measured results also demonstrate that increasing the number of amplification stages leads to a proportional enhancement in gain. Extending the design to a three-stage topology, a configuration employing CS topology in all three stages attains a gain of 27.9 dB and a 3-dB bandwidth of 25.8–30.1 GHz, again with the same NF of 3.6 dB. Using a cascode structure in the third stage enhances the gain to 29.2 dB, with a slightly reduced bandwidth of 26.1–29.8 GHz, without degrading noise performance. These results validate the expectation from the Friis formula: the overall NF is predominantly influenced by the first stage, whereas the total gain scales with the number of stages.

From an architectural perspective, the common-source topology offers simplicity, wider bandwidth, and lower power consumption, making it favorable for broadband applications. In contrast, the cascode topology provides higher gain and improved reverse isolation due to enhanced output resistance and better high-frequency performance at the cost of increased design complexity and potentially reduced bandwidth. The selection between CS and cascode thus involves a trade-off between gain enhancement and bandwidth or layout efficiency.

6. Review and reflections

In this project, we experienced for the first time the complete workflow from literature review and specification planning to circuit simulation using ADS. Initially, we lacked experience in designing millimeter-wave LNAs, but through discussions with our advisor and senior mentor, we gradually clarified our direction and learned how to fairly evaluate the performance of different topologies and adjust design parameters accordingly.

One of the biggest challenges during the simulation process was inter-stage matching and stability analysis, especially in the three-stage architectures where we needed to balance gain stacking and linearity. This journey not only enhanced our practical skills in high-frequency circuit design, but also deepened our understanding of the gap between theoretical design and real-world implementation.

Although we were not able to proceed to layout and tape-out due to time constraints, this project laid a solid foundation for future chip implementation. It also strengthened our abilities in teamwork, collaboration, and technical integration.

Finally, we would like to express our sincere gratitude to 劉怡君老師 and 莊珮綺學姊 for their generous support and encouragement. Their guidance and advice played a vital role in the successful completion of our project and significantly enhanced our academic growth.

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