



Galvanically Isolated Gate Driver for Gallium Nitride Power HEMT with Combined Power and Signal Transmission

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Abstract

Gallium Nitride (GaN) is an advantageous wide-band-gap material for high-voltage and high-frequency power electronics applications, offering low on-resistance and input capacitance. In this project, a novel frequency modulation gate driving scheme is developed. Conventional galvanically isolated gate drivers require an isolated voltage supply for the secondary side of the driver IC. We eliminate this requirement by combining the power and signal transmissions within the driver.

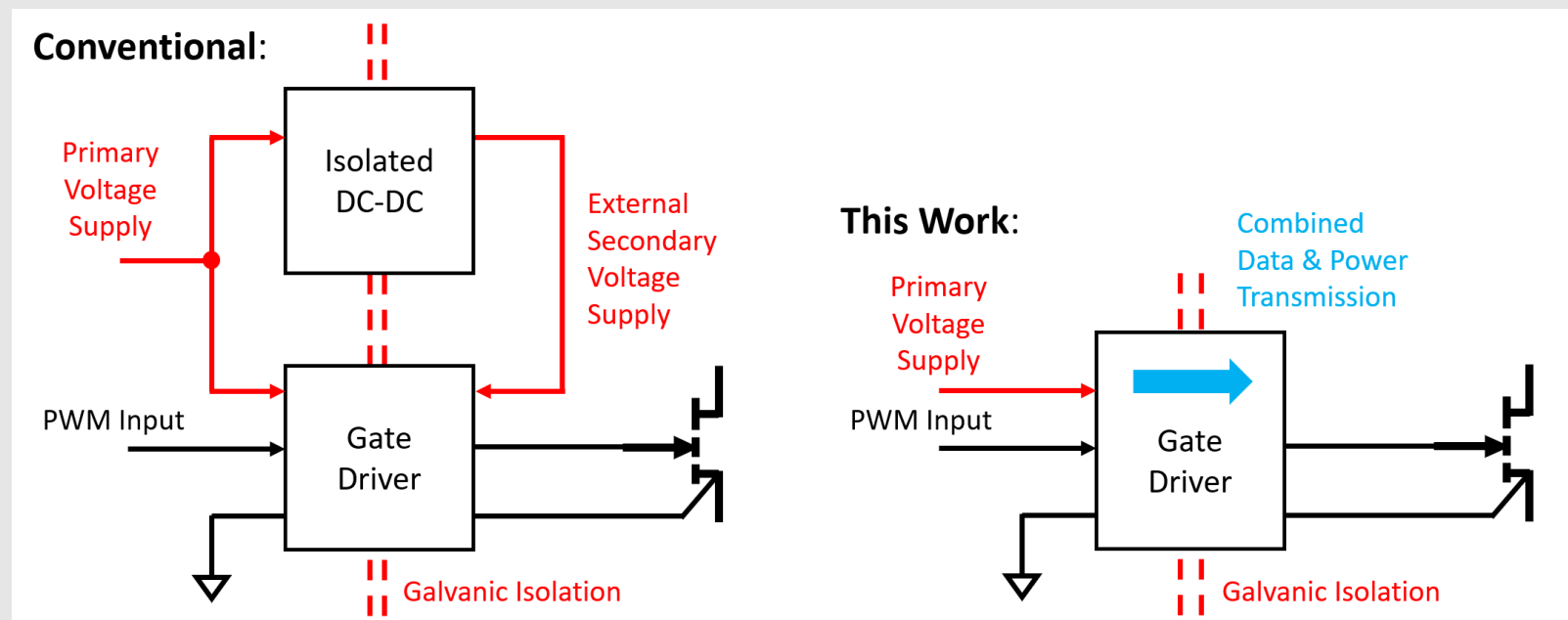


Figure 1. Comparison between conventional galvanically isolated gate driver and the proposed gate driver in this project.

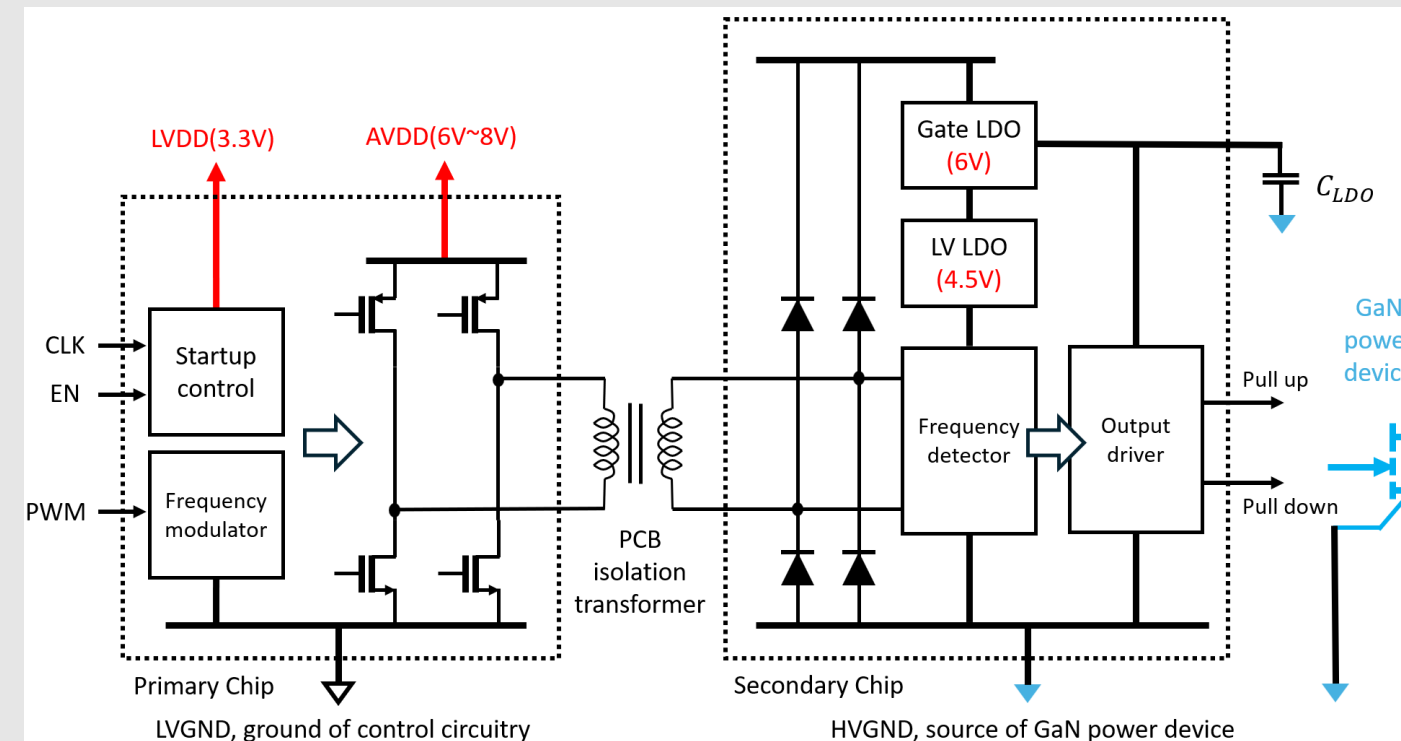


Figure 2. The architecture of the proposed gate driver.

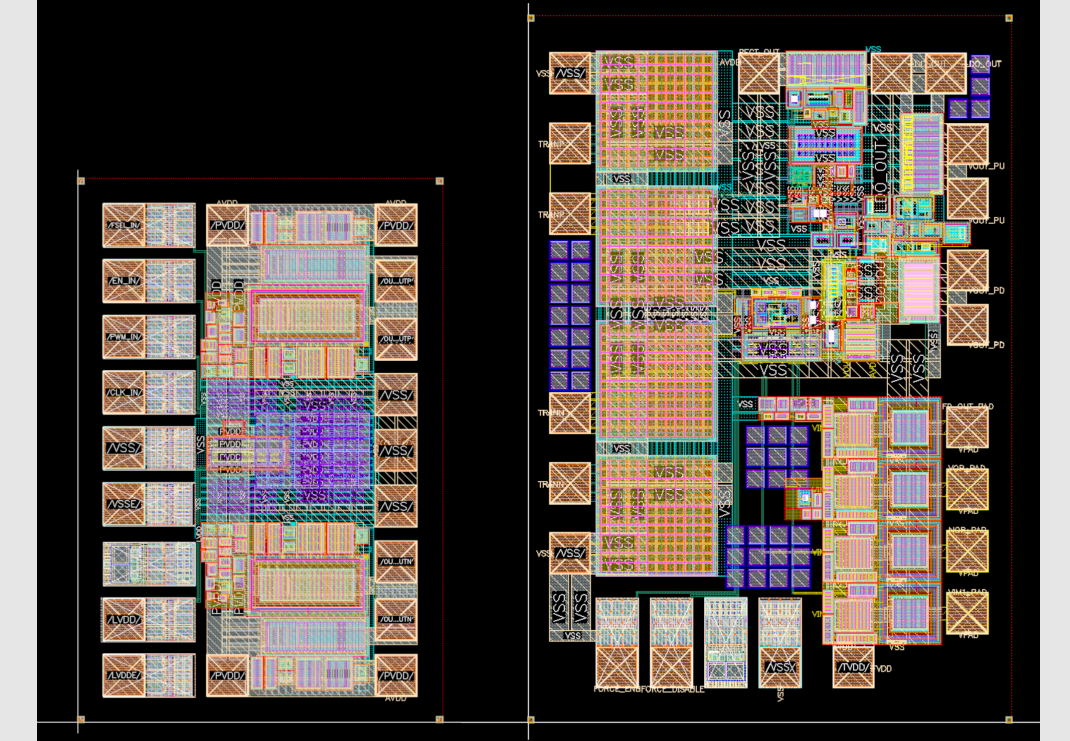


Figure 3. The layout of the primary chip (left, $654\mu\text{m} \times 976\mu\text{m}$) and secondary chip (right, $890\mu\text{m} \times 1300\mu\text{m}$).

Novel FM Gate Driving Scheme

Literature report two gate driving schemes with combined power and signal transmission: on-off keying (OOK) [1], [2] and amplitude modulation (AM) [3]. In both schemes, the oscillation in the transformer is rectified to form the power supply for the secondary side. However, both schemes suffer from varying secondary supply voltage during operation. To provide a platform for future gate driving optimization development, a stable power supply for the secondary chip is desired.

We propose a gate driving scheme based on frequency modulation to provide a stable and integrated power supply. We encode $\text{PWM} = 1$ as high frequency and $\text{PWM} = 0$ as low frequency. The low frequency is the high frequency divided by 2 with a flip-flop. The signal is demodulated by the frequency detector in the secondary chip, while power for the secondary chip is obtained by rectifying the oscillating waveform.

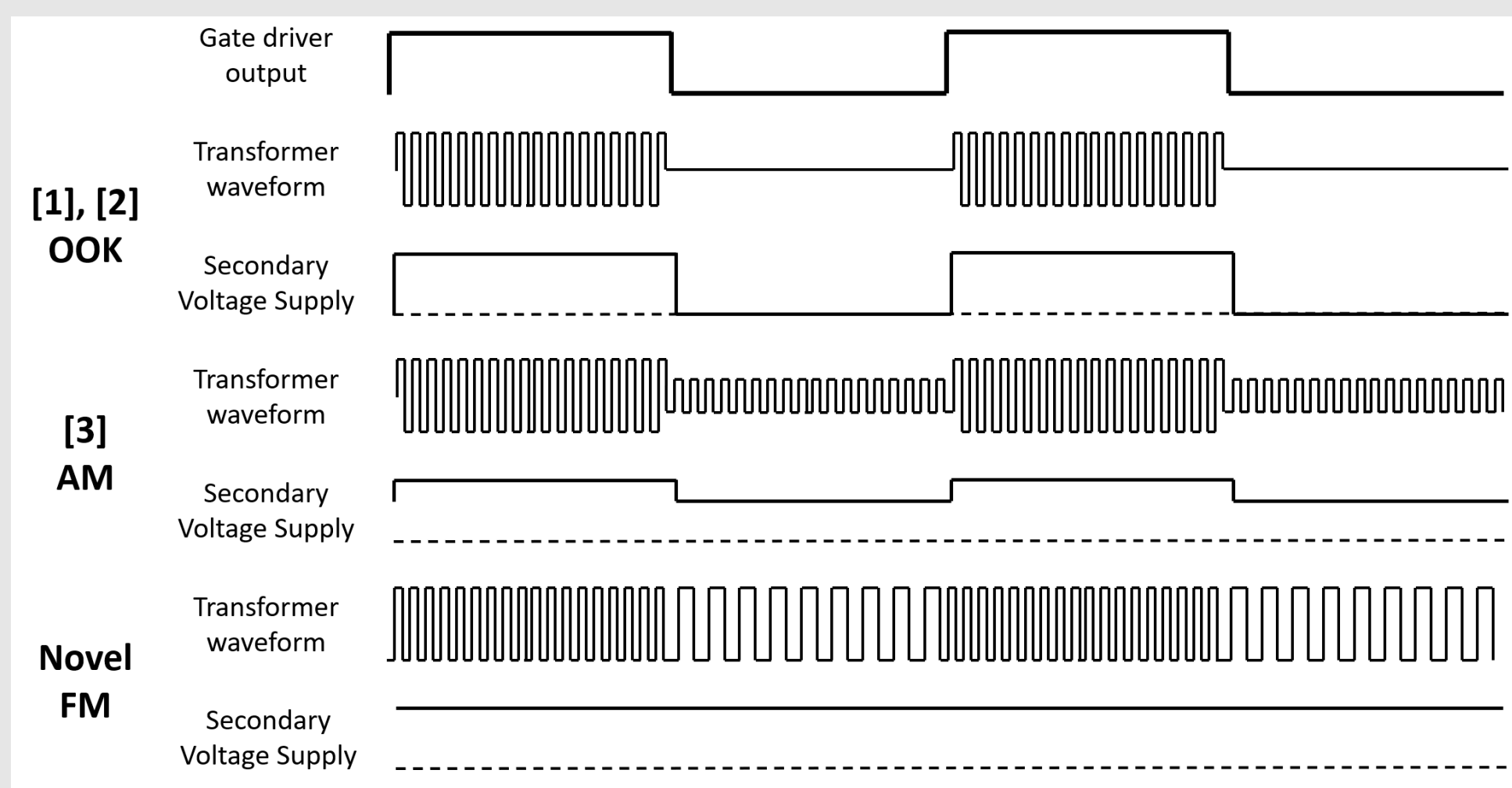


Figure 4. Comparison between gate drivers with combined power and signal transmission in literature and the proposed FM scheme.

Frequency Detector Design

The frequency detector is located on the secondary chip. It takes the signal with varying frequency from the transformer, detects the current frequency, and produces a digital demodulated signal.

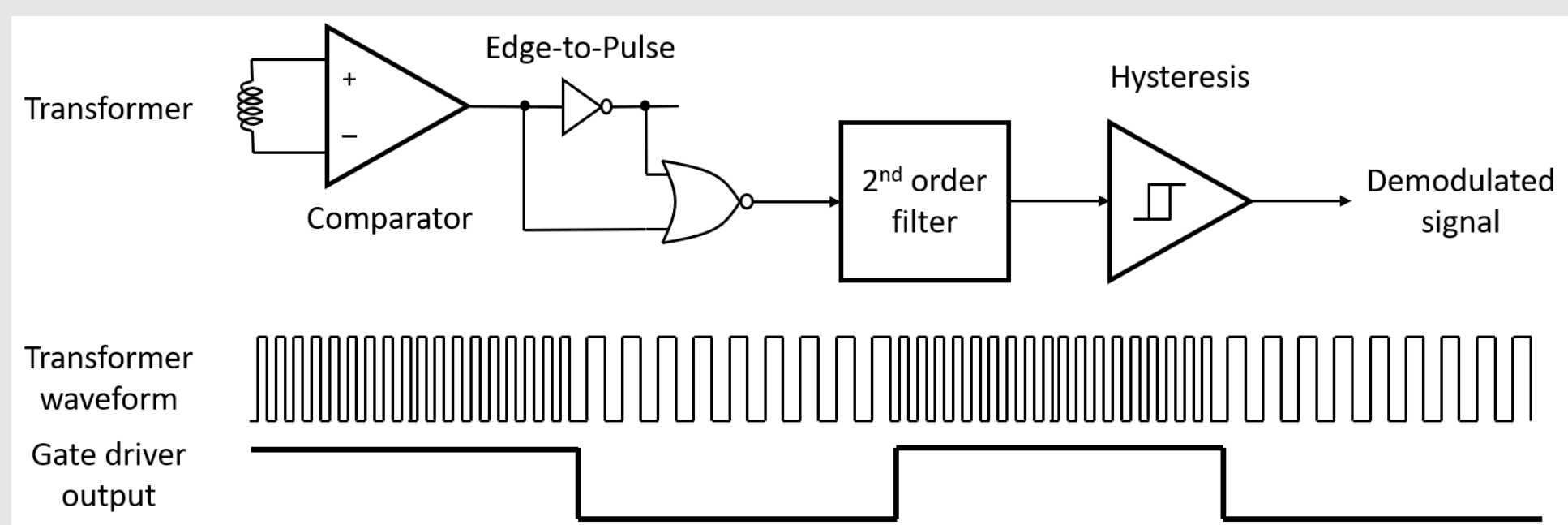


Figure 5. The block diagram of the frequency detector.

The comparator produces a clean square signal at the same frequency as the signal in the transformer by comparing the voltages at the two terminals of the secondary winding. The edge-to-pulse circuit takes the square wave and generates a pulse with fixed duration at every falling edge. The average voltage of the pulse signal will be inversely proportional to the frequency.

The 2nd-order filter is the solution to one of the major challenges in this project. The ratio between the oscillating frequency in the transformer and the target frequency of the gate drive signal is around 50 times, which cannot be adequately filtered by a simple RC low-pass filter. Therefore, we design a 2nd-order Sallen-Key filter, which provides faster roll-off and we can set a higher cut-off frequency to preserve the gate drive signal. Furthermore, we design this filter to be under-damped to make the response to frequency change faster. The hysteresis module [4] further removes the ripples and overshoot in the filter output.

Results and Conclusion

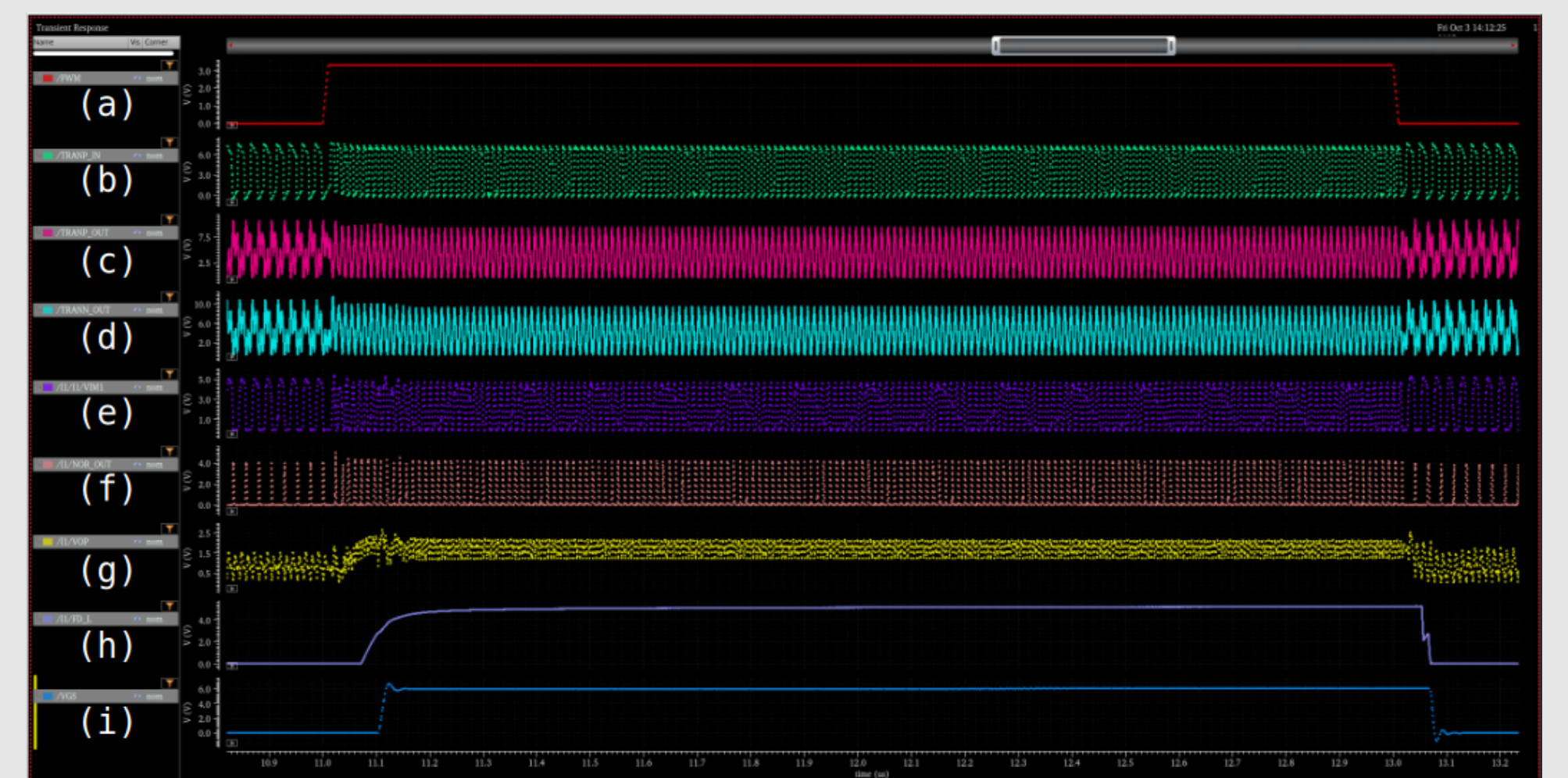


Figure 6. The pre-layout simulation results of the proposed gate driver.

The circuit is simulated at a PWM frequency of 250kHz. (a) is the PWM input and (b) is the frequency modulated output. (c) and (d) are the two terminals of the secondary winding, they are distorted due to the frequency response of the transformer. However, with the comparator, we can retrieve a clean square signal (e) for frequency detection. The square signal is then converted to a pulse signal (f). The 2nd-order filter takes the average of the pulse signal and produces signal (g), whose local average depends on the input frequency. Finally, the hysteresis circuit converts the noisy filter output (g) into a digital signal (h) and the output driver drives the gate (i) of the GaN power device.

Corner	TT	FF	SS	SF	FS
Rise time (ns)	6.47	6.64	9.48	4.82	10.63
Rise delay (ns)	136	77	155	116	105
Fall time (ns)	4.45	3.45	6.00	4.41	4.07
Fall delay (ns)	63	42	77	63	72
Power (mW)	323	400	282	318	321

Table 1. The post-layout simulation results of the proposed gate driver.

In conclusion, this project developed and implemented a novel gate driving scheme based on frequency modulation for GaN power devices. We successfully combined the power and signal transmission into the gate driver, eliminating the need for an external isolated supply. We are also able to provide a stable supply voltage for the secondary chip. The completed gate driver IC was simulated at a switching frequency of 250kHz and could achieve a worst-case minimum rise/fall time of 10.63ns when driving a 1nF load. The finished designs were submitted in October 2025 and had been approved for tape-out by TSRI. The manufactured chips are scheduled to arrive in February 2026 for testing.

References

- [1] Kenneth Kin Leong et al. "CT-Drive – A Simple Two Dice Solution Coreless Transformer Driver for Integrated GaN GIT Devices". In: *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. May 2023, pp. 1–5.
- [2] Michael Basler et al. "Monolithically Integrated and Galvanically Isolated GaN Gate Driver". In: *IEEE Open Journal of Power Electronics* 6 (2025), pp. 144–149. ISSN: 2644-1314.
- [3] Jorge Garcia et al. "Self-supplied isolated gate driver for SiC power MOSFETs based on bi-level modulation scheme". In: *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. Oct. 2017, pp. 5101–5106.
- [4] Mohammad R Hoque and Simon S Ang. "A CMOS Under-voltage Lockout Circuit". en. In: (2008).