A 8-bit 30MS/s 4 Channel Time-Interleaved SAR ADC with Togglable 3 Effective Channel Random Interleaved Sampling Method

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Abstract

A good ADC should possess both high speed and low power. However, for Successive Approximation Register Analog-to-Digital Converters (SAR ADCs), achieving low power comes at the cost of longer conversion time, because for each output bit in a single data point, the conversion requires the comparison and CDAC settling time. When the operating speed of the SAR ADC approaches the process limit, it becomes quite challenging to balance the speed and power.

Therefore, in this project, we employ a Time-Interleaved (TI) architecture that allows four channels of SAR ADC to operate in parallel. Even though the operating speed of each channel is still limited by the process, effectively, this approach overcomes that limitation, enabling the overall ADC to quadruple the maximum operating frequency of a single-channel SAR ADC while maintaining the same resolution.

Interleaving improves the FOM because, as the conversion speed of a single channel approaches the limits of the technology, the power-speed tradeoff becomes nonlinear, demanding a disproportionately higher power for a desired increase in speed. For example, op amps and comparators eventually reach diminishing returns in their speed as their power consumption is raised. From another perspective, each ADC architecture incurs a certain "timing overhead" that does not easily scale with power.

Moreover, Recent high-speed ADCs, especially for communication applications, require higher sampling rates with wide spurious free dynamic range (SFDR). To achieve high sampling rate, a TI ADC architecture is quite popular and recently can be seen in many papers. However, it is also well known that spurious components occur when using the conventional interleaved sampling method, if the mismatch between each channel exists. These spurious components seriously degrade the SFDR.

This project implements the Random Interleaved Sampling (RIS) Method, so that we can spread the spurious components into noise level and get better SFDR. The Conventional Interleaved Sampling Method is also implemented for comparison, and the Timing Mismatch Calibration is taken to control or purposely increase the channel mismatch for showing the effectiveness of RIS Method.

1. Introduction

The Successive Approximation Register Analog-to-Digital Converter (SAR ADC) is a widely used type of analog-to-digital converter known for its low power consumption, small area, and medium-to-high resolution. Its operation is based on comparing the output voltage of a Digital-to-Analog Converter (DAC) with a comparator. It takes the Binary Search Algorithm to obtain the digital output for each bit successively.

However, for SAR ADCs, after each comparison, there is a need to switch the DAC based on the comparison result, followed by providing sufficient settling time for the DAC's output to stabilize before the next comparison occur. Moreover, an N-bit SAR ADC requires repeating the above process N times to complete the conversion of a single data point. Therefore, the maximum operating speed of SAR ADCs is often limited by the DAC and resolution, which is a notable drawback.

To improve the maximum operating speed of SAR ADCs, one approach is to employ a time-interleaved (TI) architecture. In the time-interleaved architecture, N identical ADCs are operated in parallel by controlling their clock signals. As a result, even though the operating speed of each ADC remains the same, the overall ADC speed can be increased N times compared to a single-channel ADC.

In this project, the T18 process is used to construct a 4-channel 8-bit time-interleaved SAR ADC. The architecture and switching method are based on the monotonic capacitor switching procedure mentioned in reference [1].

For the SAR ADC, the monotonic capacitor switching procedure is utilized for DAC switching, where only the bottom plate of one capacitor is switched after each comparison. The advantage of this approach is that it further reduces the power consumption required for SAR ADC conversion. However, a drawback is that the input common-mode voltage of the comparator gradually converges to 0V during the successive comparisons. Therefore, this architecture has higher design requirements on the comparator over noise and mismatch rejection under different input common-mode voltages, and thus ensuring the accuracy of the output results.

Moreover, Recent high-speed ADCs, especially for communication applications, require higher sampling rates with wide spurious free dynamic range (SFDR). To achieve high sampling rate, a TI ADC architecture is quite popular and recently can be seen in many papers. However, it is also well known that spurious components occur when using the conventional interleaved sampling method, if mismatch between each channel exists. These spurious components seriously degrade the SFDR.

This project implements the Random Interleaved Sampling (RIS) Method in reference [2], as showed in Fig. 1. So that we can spread the spurious components into noise level and get better SFDR. The Conventional Interleaved Sampling Method is also implemented for comparison, and the Timing Mismatch Calibration, is taken to control or purposely increase the channel mismatch for showing the effectiveness of RIS Method. In this project, the RIS Method is with 3 effective channel and 4 total channel (1 extra channel), and the Conventional Method is with 4 total channel.

Through circuit simulations, the operating speed of the single-channel SAR ADC was set to be 10 MS/s, thus the three effective channel time-interleaved SAR ADC achieves the expected operating frequency of 30 MS/s while maintaining the resolution of the single-channel SAR ADC.

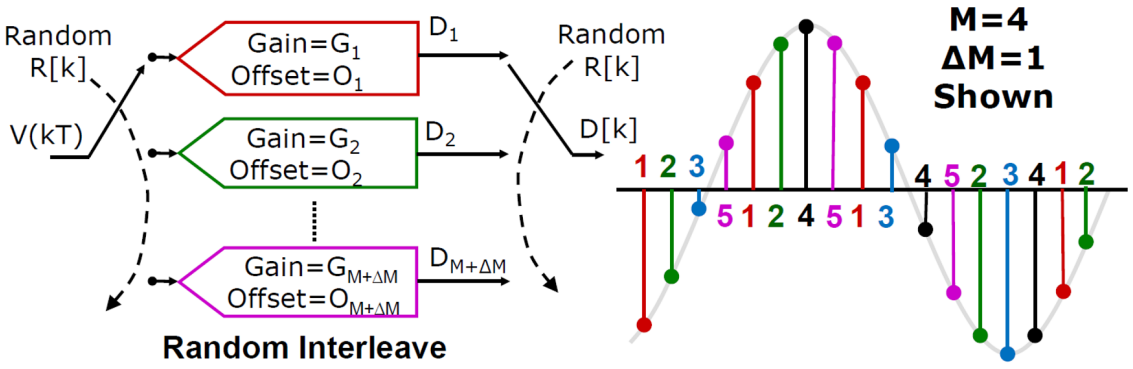


Fig. 1. The Random Interleaved Sampling (RIS) Method to smear the spurious components by randomness, when channel mismatch exists

2. Block diagrams and operating principles

This project consists of a CLK generator, a pseudo random bit sequence (PRBS) circuit for the RIS method, 4 single-channel SAR ADCs, and the MUXs; with differential input, sampling clock, a control signal to toggle RIS/Conventional method, and 8 bit digital outputs, as showed in Fig. 2.

Each single-channel SAR ADC includes circuits such as Sample & Hold, Comparator, CDAC (Capacitor Array), Asynchronous Control Logic, and DAC Control, as showed in Fig. 3.

The operation of a single-channel SAR ADC is as follows: the differential input is fed into the Sample & Hold circuit, which samples the input data based on the clock signal. The sampled data is then applied to the top plate of the DAC and connected to the Comparator. The Comparator compares the voltage levels of the positive (P) and negative (N) inputs. After the comparison, the Comparator outputs the result to the DAC Control circuit. Based on the comparison result, the DAC Control circuit switches the bottom plate of the first capacitor in the CDAC and outputs the result of the first bit. The voltage held on the top plate of the CDAC is hence subtracted proportionally based on the capacitor ratios, then the comparison of the first bit is completed. This process is repeated until the comparison of the 8th bit (LSB) completed, gradually approximating the total 8-bit output codes.

The Asynchronous Control Logic serves the purpose of transmitting clk1 to clk8 to the DAC Control circuit after each comparison is completed by the Comparator. This allows the DAC Control circuit to switch the corresponding capacitor's bottom plate based on the current comparison result.

In this design, the Time-Interleaved ADC architecture is used, which includes four channels of SAR ADCs. The CLK generator output is the randomly or sequentially interleaved CLKs1 to CLKs4, based on the control signal RIS on/off, and the generated four CLKs serve as the clock signals for Channel 1 to Channel 4, respectively. In the end, the output 8-bit data of 4 channels are also interleaved accordingly, by the 4:1 MUX, to become the final 8-bit output codes.

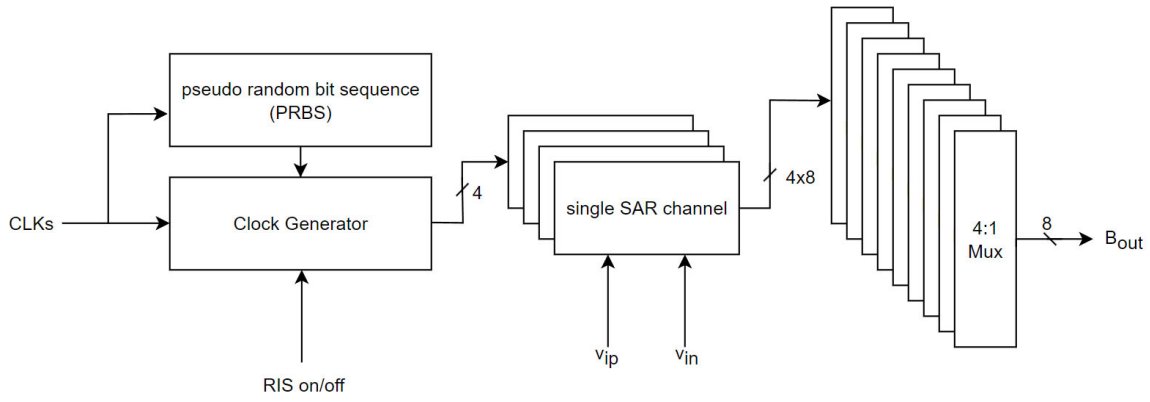


Fig. 2. The overall block diagram of this project

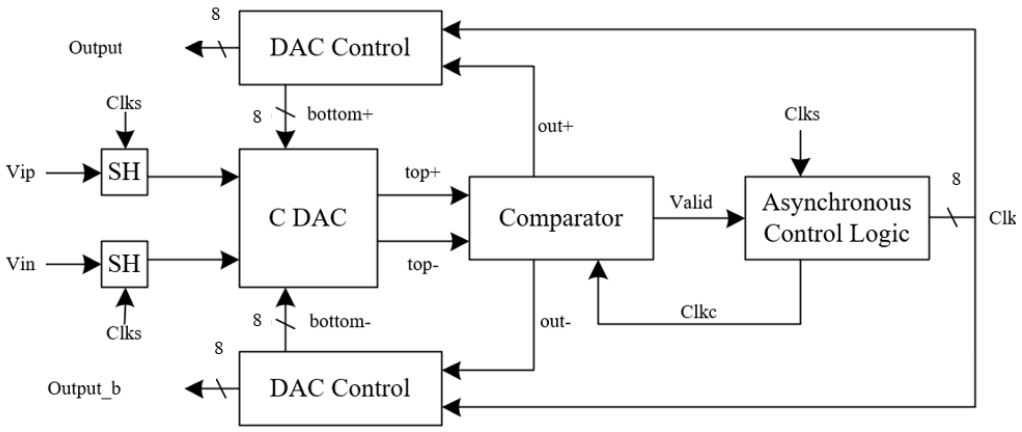


Fig. 3. The block diagram of single channel SAR ADC

3. Simulation results

TI-SAR result (256 points of FFT, Nyquist rate input)

Pre-sim

Corner (25℃)	ENOB (bits)	SFDR (dB)
RIS on		
TT	8.115	60.982
FS	8.076	61.237
SF	8.123	61.232
FF	8.028	61.521
SS	8.085	61.656
RIS off		
TT	8.115	60.982
FS	8.076	61.237
SF	8.123	61.232
FF	8.028	61.521
SS	8.085	61.656

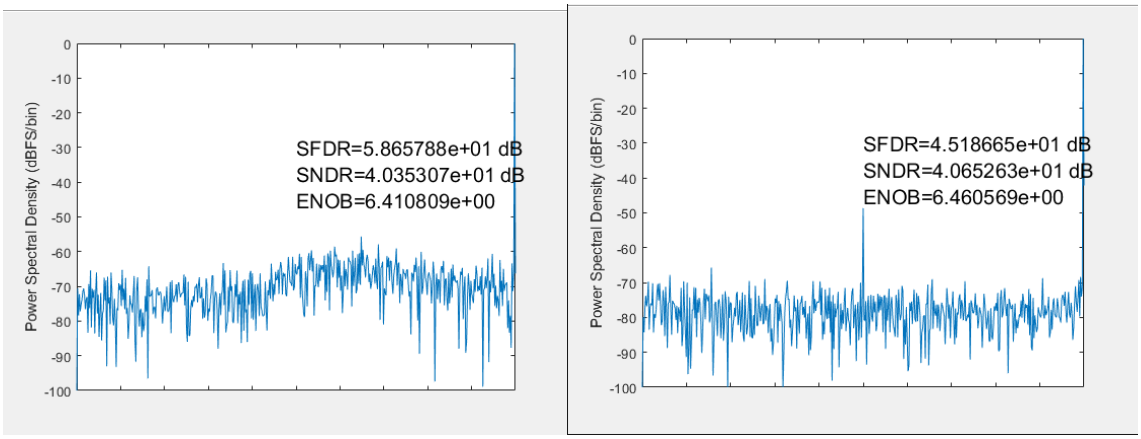
Post-sim

Corner (25℃)	ENOB (bits)	SFDR (dB)
RIS on		
TT	7.732	61.490
FF	7.909	62.236
SS	7.850	61.537

RIS off		
TT	7.702	60.853
FF	7.930	61.843
SS	7.866	61.427

As showed in the tables above, all simulated ENOB are larger than 7.7bits. Also, there are no mismatch between each channel at pre-sim, hence the simulation results of RIS on/off are exactly the same; in contrast, the SFDR is increased by the RIS method at post-sim, due to the existence of channel mismatch.

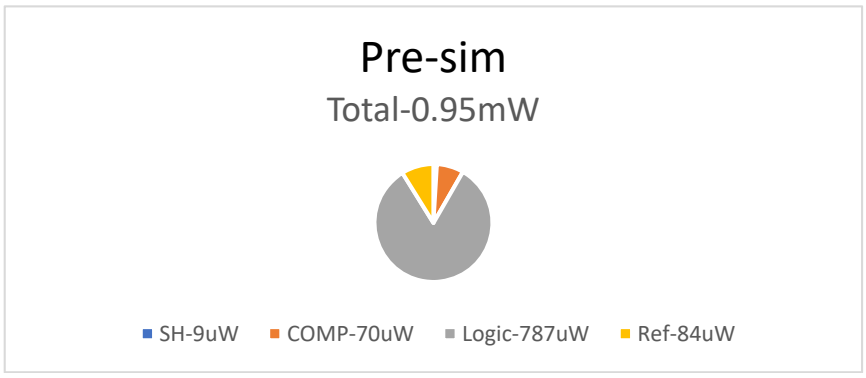
To further demonstrates the effectiveness of RIS method, we purposely add a timing mismatch between each channel, with the analog timing calibration. In Fig. 16., the great SFDR boosting of RIS method is clearly showed, the idle tone in (b) is spread over the noise level, as in (a). Even though the noise level in (a) is not 'white', owing to the incomplete randomness in this project (3 effective channel instead of 1, and the PRBS), the SFDR still achieves a decent value under large channel mismatch.

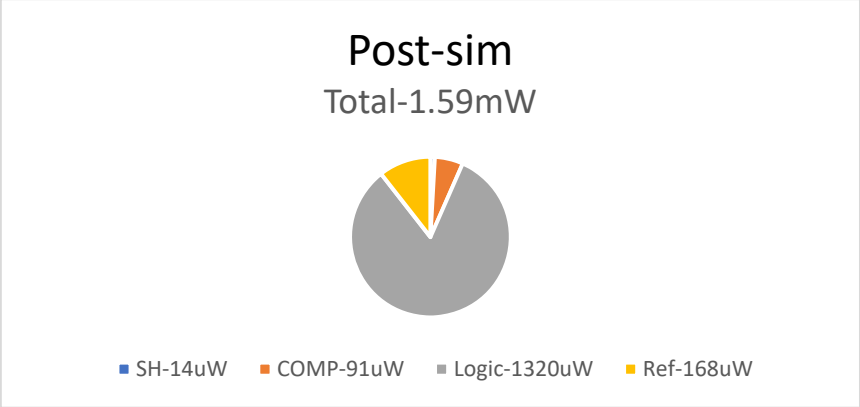


(a) (b)

Fig. 4. The spectrum with purposely added timing mismatch (a) RIS on(b) RIS off

Power Breakdown of TI-SAR





SH: sample and hold circuit,

COMP: comparator,

Logic: digital logic,

Ref: reference voltage (For DAC switching)

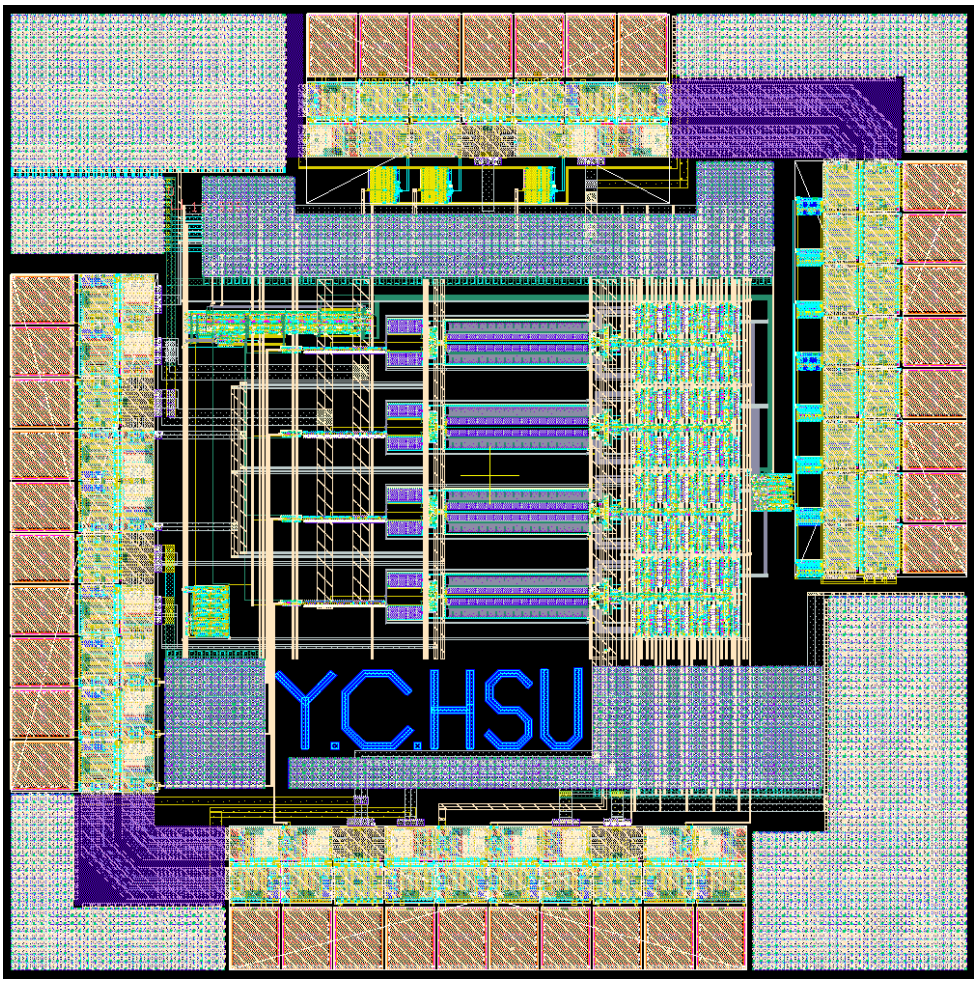
As showed above, almost all power is 1.6x at post-sim, because the enormously increased parasitic capacitance loading.

Except the comparator power, which is increased only about 1.3x, because its power is dominated by the current mirror biased tail current, especially the short circuit current in the period between the completion of comparison and the clock reset phase. However, such period is needed to prevent the meta-stability of comparator, and the resulting ENOB drop, at certain input voltage.

Also, the power of reference voltage is doubled instead of 1.6x, because in the CDAC array, a lot of capacitance not only exists between bottom-plate and top-plate, but also between each bottom-plates, which significantly increases the loading of DAC control circuit, the reference voltage switch.

4. Layout

Chip Size: 1200×1200 $\boldsymbol{um^2}$
Pin number: 35



5. Conclusion

This project implemented a 4 channel 8-bit Time-Interleaved SAR ADC using the T18 process. Simulation results confirmed that this architecture could triple the maximum operating frequency (when RIS on) compared to a single-channel SAR ADC while maintaining the 8-bit resolution, increasing it from 10MS/s to 30MS/s. Due to area and circuit complexity constraints, this project focused on a 4 channel TI architecture; however, utilizing more channels could further increase the operating speed.

Moreover, the mismatch between each channel due to process variation is an obstacle that limits the performance of TI ADC, especially the timing mismatch (clock skew), which is hard to be perfectly calibrated. Through the RIS method, the SFDR is proven boosted significantly even under large timing mismatch.

However, the RIS method can't increase the ENOB, the TI ADC still suffers from channel mismatch in terms of resolution, SNDR. Also, the digital circuits for RIS operation is very

power consuming, comparing to the low power SAR ADC channel, which contradicts to the FOM-benefit property of TI architecture. Besides, the demand of extra spare channel slows the TI ADC down slightly, which is also a non-negligible drawback when the number of channels is small.

6. References

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[6] Yuan Zhou, Benwei Xu, Yun Chiu, "A 12-b 1-GS/s 31.5-mW Time-Interleaved SAR ADC With Analog HPF-Assisted Skew Calibration and Randomly Sampling Reference ADC" in IEEE Journal of Solid-State Circuits, VOL. 54, NO. 8, April 2019 DOI: 10.1109/JSSC.2019.2915583

7. Review and reflections

Although We had prior experience of circuit design in courses such as VLSI and AIC, it was only after starting this project that We realized the exercises in those classes were just foundational. Designing a circuit for actual fabrication involves considering the impact of corners, power supply, temperature on performance, as well as incorporating non-ideal effects like noise, mismatch, clock jitter, coupling, and more. Therefore, the design process was much more challenging than the assignments We had undertaken before.

In addition, this project marked our first experience creating the layout for an analog circuit and our first time senting a chip to fabrication. However, we learned numerous layout techniques and concepts, such as using Guard Ring or Shielding to protect analog circuits and sensitive signals, understanding the role and application of dummy cell, and considerations and planning for I/O PADs. Over the past few months, from paper survey to the final chip measurment, we believe we've made significant progress in our ability about circuit design.

Finally, we would like to express our gratitude to each other teammates, for the assistance during this period, working together to accomplish the project tasks. We are thankful to the senior students in the lab who sacrificed their research time to help us overcome various difficulties encountered during the project. Special thanks to our advisor for designing such a rigorous project training, providing guidance in each meeting, allowing us the opportunity to personally experience the entire process of Fullcustom design flow, and enhancing our capabilities.