A 8-bit 30MS/s 4 Channel Time-Interleaved SAR ADC with Togglable 3 Effective Channel Random Interleaved Sampling Method

具有可開關式三等效通道隨機交錯取樣方法之每秒三千萬次採樣之四通道八位元時序交錯式循序漸進類比數位轉換器

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Abstract

Recent high-speed ADCs, especially for communication applications, require higher sampling rates with wide spurious free dynamic range (SFDR). To achieve high sampling rate, a TI ADC architecture is quite popular. However, it is also well known that spurious components occur when using the conventional interleaved sampling method, if the mismatch between each channel exists. These spurious components seriously degrade the SFDR. This project implements the Random Interleaved Sampling (RIS) Method, so that we can spread the spurious components into noise level and get better SFDR.

Operating Principles

Fig. 1. is the block diagram of the TI ADC we implemented. The clock generator output is the randomly or sequentially interleaved CLKs1 to CLKs4, based on the control signal RIS on/off, and the generated four CLKs serve as the clock signals for channel 1 to channel 4. In the end, the output 8-bit data of 4 channels are also interleaved accordingly, by the 4:1 MUX, to become the final 8-bit output codes.

Each single-channel SAR ADC is showed in Fig. 2. Input data is first sampled by SH circuit, on the top-plate of CDAC, the comparator then compares the voltage of the P and N side. After each comparison, the comparator outputs the result to the DAC control circuit, the bottom plate of a certain capacitor in the CDAC would be switched to feedback the comparison result into the top plate. The voltage held on the top plate is hence subtracted proportionally based on the capacitor ratios, this process is repeated until the comparison of the 8th bit (LSB) completes, gradually approximating the total 8-bit output codes. The asynchronous control logic serves the purpose of transmitting Clk1 ~ Clk8 to the DAC control circuit.

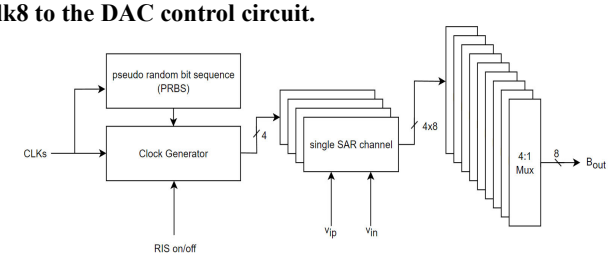

Fig. 1. The overall block diagram of this project

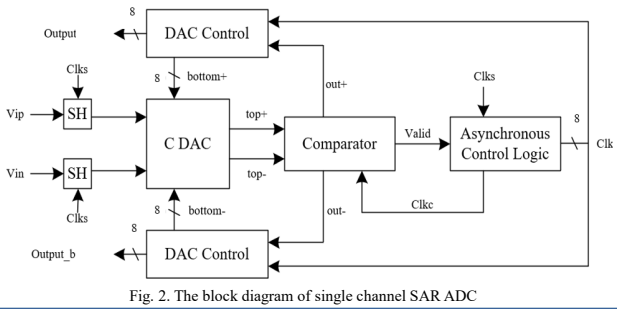

Fig. 2. The block diagram of single channel SAR ADC

Interleaving methods

Fig. 3 depicts two interleaving methods. Conventional method choses each channel sequentially, multiplies the sampling rete fs with the number of total channels. RIS choses spare channels randomly, multiplies fs with the effective channel numbers (channels in use simultaneously), while spreading the spurious components by randomness.

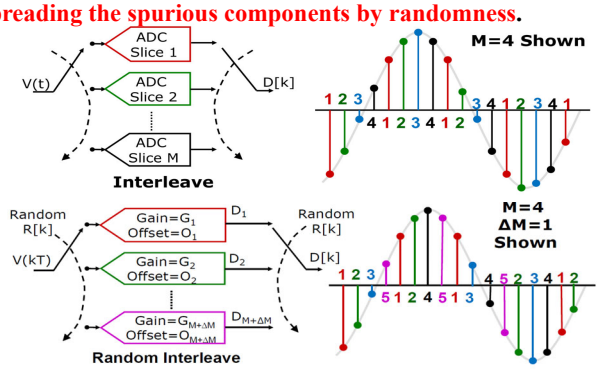

Fig. 3. The Conventional Time-Interleaving (TI) and Random Interleaved Sampling (RIS) Method

Results

Table. 1, Fig. 5 shows the SFDR boost of RIS method.

Corner (25℃)	ENOB (bits)	SFDR (dB)
RIS on		
TT	7.732	61.490
FF	7.909	62.236
SS	7.850	61.537
RIS off		
TT	7.702	60.853
FF	7.930	61.843
SS	7.866	61.427

Table. 1. The Post-sim performance (Nyquist input)

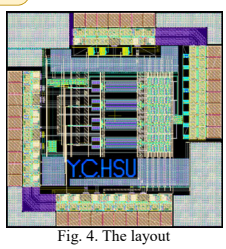

Fig. 4. The layout

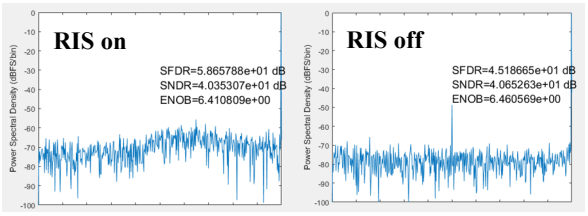

Fig. 5. The FFT spectrum, with purposely added timing mismatch, for RIS on/off

Conclusion

The mismatch between each channel due to process variation is an obstacle that limits the performance of TI ADC, especially the timing mismatch (clock skew), which is hard to be perfectly calibrated. Through the RIS method, the SFDR is proven boosted significantly even under large timing mismatch.

However, the RIS method can't increase the ENOB, the TI ADC still suffers from channel mismatch in terms of resolution, SNDR. Besides, the demand of extra spare channel slows the TI ADC down slightly, which is also a non-negligible drawback when the number of channels is small.

Reference

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