Spiking Neural Network FPGA Accelerator

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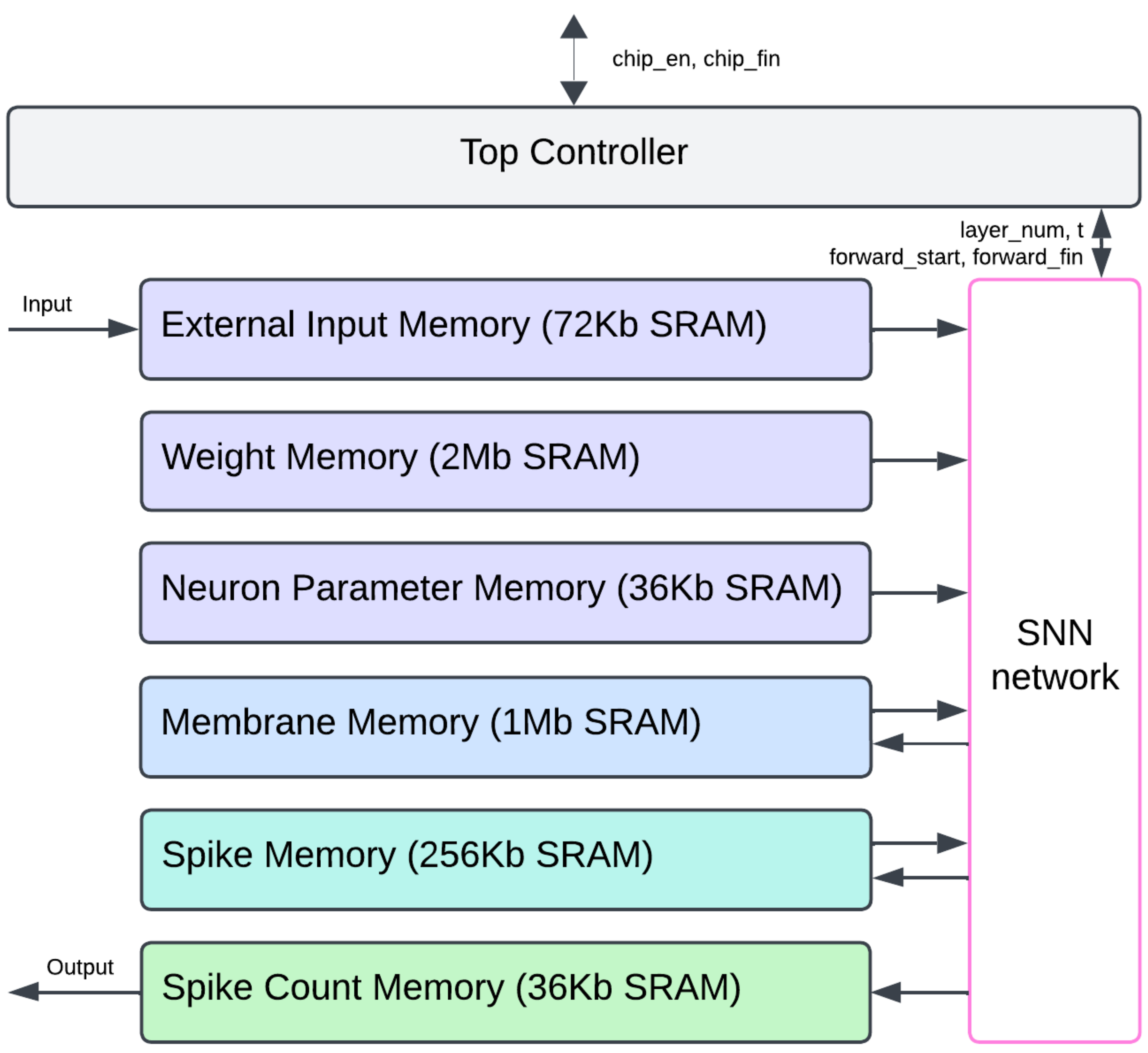
Traditional spatial recognition algorithms typically require substantial computational resources. However, Spiking Neural Networks (SNNs) optimize the spatial recognition process by mimicking the unique ability of insects to perceive space with a minimal number of neurons. Their low latency, reduced computational requirements, and low power consumption make SNNs highly promising for such tasks. This research focuses on utilizing hardware-friendly neurons based on the Integer Quadratic integrate-and-fire (IQIF) neuron model and implements the system using a PYNQ board and a webcam for applications.

SNN Accelerator

5 network layers with 704 IQIF neurons
External input: Angular velocity, optical flow, velocity are external input for layer1, 2, 4 respectively
Forwarding for 100 timesteps: To generate depth data for a single frame, the SNN accelerator performs 100 forward passes.
Integer parameter: The neuron parameters for the IQIF neurons and the weights between neurons in different layers are all integers ranging from -127 to 128, making the design hardware-friendly.
Conserved hardware resource: Five network layers use one shared network resource to reduce hardware burden.
Memory usage: Access weight, neuron parameter and temporary data from memory



Integer Quadratic Integrate & Fire Neuron (IQIF)

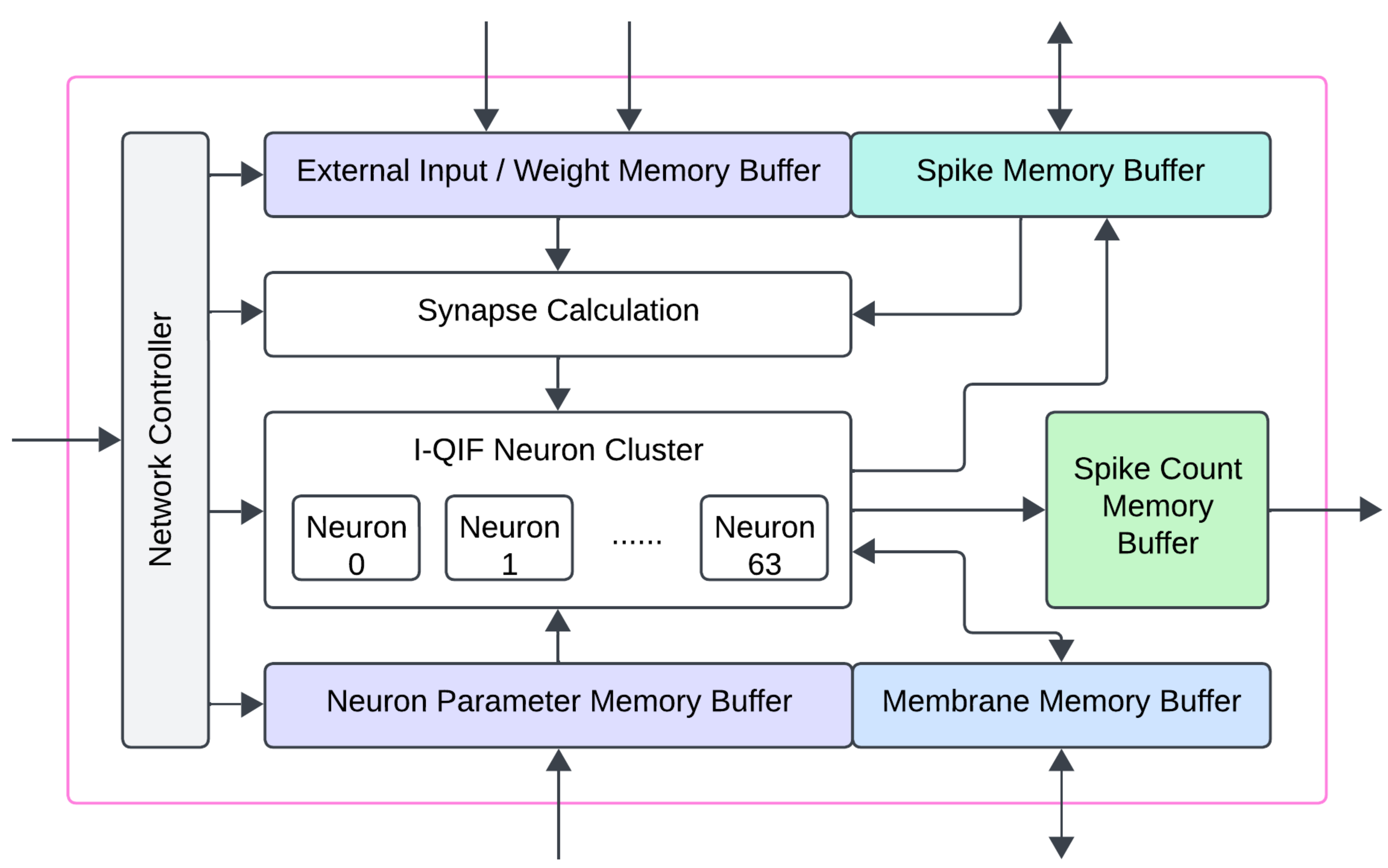
By using hardware-friendly integer arithmetic, the quadratic integrate-and-fire (IQIF) neuron model is implemented for accumulating spikes. Compared to LIF neurons, IQIF neurons can achieve more spiking activity while using a smaller circuit area. Additionally, by linearizing the partial differential equations governing membrane potentials, the computational complexity is reduced, and processing speed is improved.

$$
\begin{cases}
I = V[t-1] + \text{Synaptic input} \quad \ldots\ldots (1) \\
V'[t] = \begin{cases} I + a * (V_{rest} - V[t-1]), & V[t-1] < V_{pdeth} \\ I + b * (V[t-1] - V_{threshold}), & V[t-1] \geq V_{pdeth} \end{cases} \quad \ldots\ldots (2) \\
V[t] = \begin{cases} V_{reset}, & V'[t] \geq V_{threshold} \quad \text{(neuron fire, emit spike)} \\ V[t], & V'[t] \leq V_{threshold} \\ 0, & V'[t] < 0 \end{cases} \quad \ldots\ldots (3)
\end{cases}
$$

Application

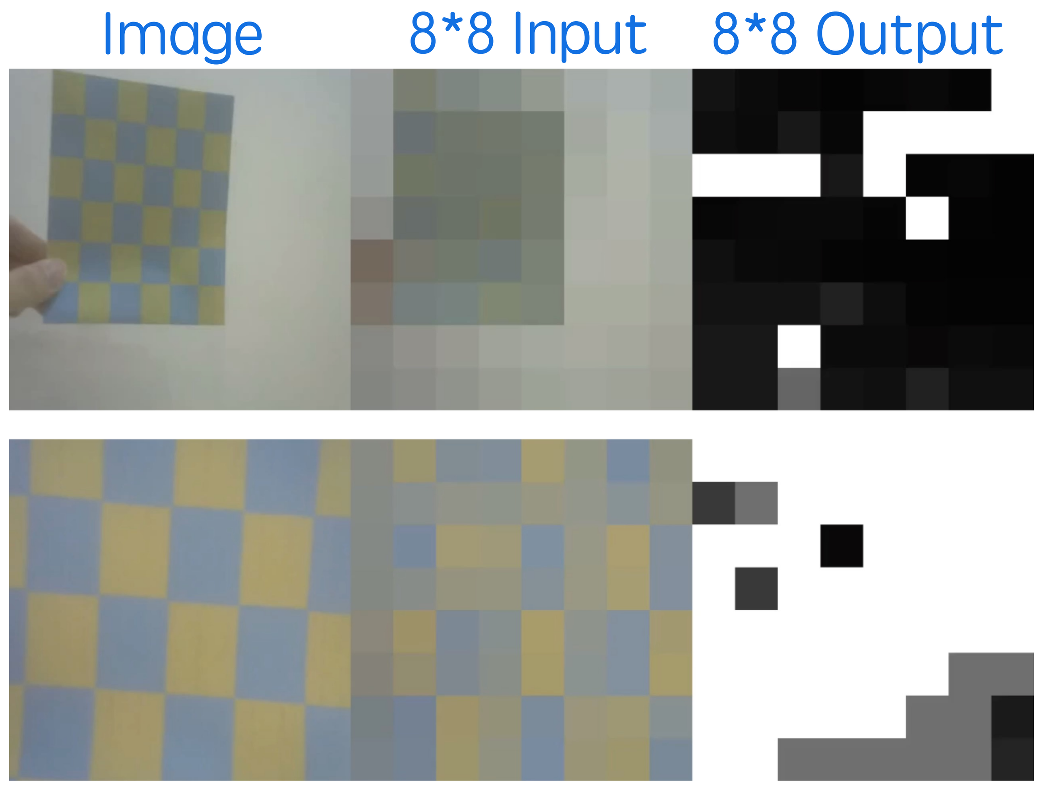
The system uses a webcam to capture input. The ARM processor on the PYNQ board handles input data pre-processing and manages output data display, while the FPGA is responsible for performing the calculation. The webcam captures the input data and sends it to the processor.

1. Webcam: The webcam captures the input image and sends it to the processor.
2. Processor: The processor downsizes the image to 8*8 resolution, then calculates the optical flow.
3. SNN accelerator: The SNN accelerator on the FPGA uses this data to compute the spatial depth between the system and the target object. Data is transferred between the processor and the SNN accelerator via the AXI4 interface.
4. Display: The calculated depth information is then displayed as a video, showcasing the SNN accelerator's application in 3D spatial depth computation.

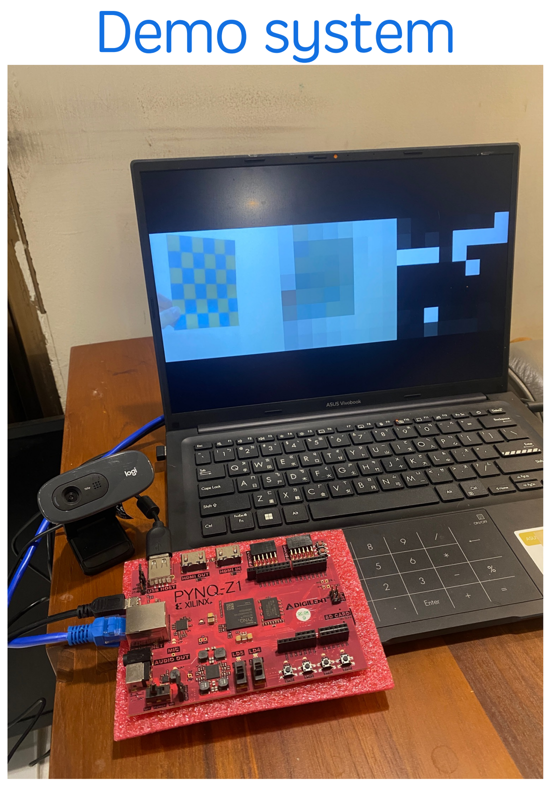


Distant objects appear darker (more black) in the image, while close objects are displayed with lighter tones.

Image 8*8 Input 8*8 Output



Demo system



Future work: Simulate angular velocity and velocity from optical flow or use camera-IMU bundle.

Reference:
Chen-Fu Yeh, Chao-Yang Tang, Tsu-Chiao Chen, et al. FlowDep - An efficient and optical-flow-based algorithm of obstacle detection for autonomous mini-vehicles. TechRxiv. April 03, 2024.
W. -C. Wu et al., "Integer Quadratic Integrate-and-Fire (IQIF): A Neuron Model for Digital Neuromorphic Systems," 2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS), Washington DC, DC, USA, 2021, pp. 1-4, doi: 10.1109/AICAS51828.2021.9458572.